BAT32G179 Datasheet

ARM® Cortex®-M0+ based, ultra low power consumption 32-bit microcontroller

Built-in 512K byte Flash, rich simulation function, timer and various communication interfaces

V1.0.6

Features

- **Ultra-low power consumption operating environment:**
  - Power supply voltage range:1.8V to 5.5V
  - Temperature range: -40℃ to 105℃
  - Low power consumption mode: sleep mode, deep sleep mode
  - Operating power consumption: 120uA/MHz@64MHz
  - Power consumption in deep sleep mode:1.5uA
  - Deep sleep mode +32.768K+RTC: 1.9uA
- **Core:**
  - ARM®32-bitCortex®-M0+ CPU
  - Working frequency: 32KHz~64MHz
- **Memory:**
  - 512KB Flash memory, with program and data storage shared
  - 20KB dedicated data Flash memory
  - 64KB SRAM memory with parity check
- **Power and reset management:**
  - Built-in power-on reset (POR) circuit
  - Built-in voltage detection (LVD) circuit (threshold voltage can be set)
- **Clock management:**
  - Built-in high-speed vibrator, accuracy (±1%). Can provide 1MHz~64MHz system clock and peripheral module operation clock
  - Built-in 15KHz low-speed oscillator
  - Built-in 1 PLL
  - Support 1MHz~20MHz external crystal oscillator
  - Support 32.768KHz external crystal oscillator, which can be used to calibrate internal high-speed oscillator
- **Multiplier/divider module:**
  - Multiplier: Support single cycle 32bit multiplication operation
  - Divider: Support 32bit signed integer division operation, only 8 CPU clock cycles to complete an operation
- **Enhanced DMA controller:**
  - Interrupt trigger start
  - Transmission mode is selectable (normal transmission mode, repeated transmission mode, block transmission mode and chain transmission mode)
  - The transmission source/destination area is optional for the full address space range
- **Linkage controller:**
  - The event signals can be linked together to realize the linkage of peripheral functions.
  - 15 types of event input, 10 types of event trigger.
- **Abundant analog peripheral:**
  - 12-bit precision ADC converter, conversion rate 1.42Msps, 28 external analog channels, internal optional PGA output as conversion channel, with temperature sensor, support single-channel conversion mode and 2, 3, 4 channel scan conversion mode Conversion range: 0 to positive reference voltage
  - 8-bit precision D/A converter, 2-channel analog output, real-time output function, output voltage range 0~V_{DD}
  - Comparator (CMP), built-in two-channel comparator with hysteresis, optional input source, reference voltage can be external reference voltage or internal reference voltage
  - Programmable gain amplifier (PGA), built-in two-channel PGA, can set 4/8/10/12/14/16/32 times gain, with external GND pin (can be used as differential mode)
- **Input/output port:**
  - Number of I/O port: 59-93
  - Can switch between N-channel open drain, TTL input buffer and internal pull-up and pull-down
  - Built-in button interrupt detection function
  - Built-in clock output/buzzer output control circuit
- **Serial two-wire debugger (SWD)**
- **Abundant timer:**
  - 16-bit timer: 17 channels (With PWM function and motor dedicated PWM function)
  - 15-bit interval timer: 1
  - Real-time clock (RTC): 1 (with perpetual calendar, alarm clock function, and supports a wide range of clock correction)
  - Watchdog timer (WWDT): 1
  - SysTick timer
- **Abundant and flexible interface:**
  - 4-channel serial communication unit: each channel can be freely configured as a 1-channel standard UART, 2-channel SPI or 2-channel simple I^2C
  - Standard SPI: 2 channels (Support 8bit and 16bit)
  - Standard I^2C: 2 channels
  - CAN:3 channel
  - LCD BUS interface: support 8080, 6800 interface

- **security function:**
  - Comply with relevant standards of IEC/UL 60730
  - Abnormal storage space access error
  - Support RAM parity check
  - Support hardware CRC check
  - Support important SFR protection to prevent misoperation
  - 128-bit unique ID number
  - Flash secondary protection in debug mode (level1: only the entire flash area can be erased, not read or write; level2: the emulator connection is invalid, and the flash operation is not possible)
- **Encapsulation:**
  - Support multiple encapsulation of 64Pin, 80Pin and 100Pin

1 Overview

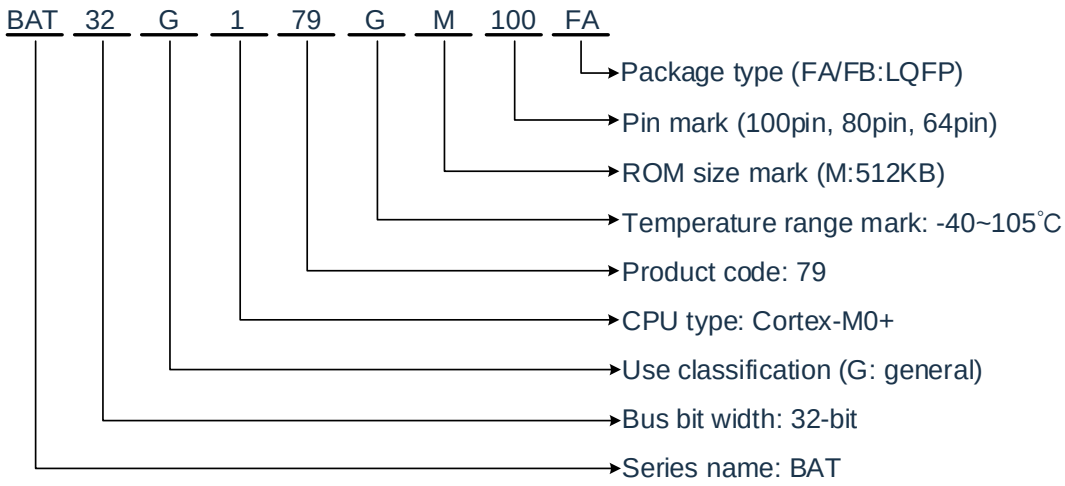
1.1 Introduction

Ultra-low power consumption BAT32G179 uses high-performance 32-bit RISC core of ARM®Cortex®-M0+, can work up to 64 MHz, and adopts high-speed embedded flash memory (SRAM max. 64KB, program/data flash memory max. 512KB). This product integrates multiple standard interfaces of I2C, SPI, UART, LIN and CAN bus Integrated 12bit A/D converter, temperature sensor, 8bitD/A converter, comparator, programmable gain amplifier. Among them, the 12bit A/D converter can collect external sensor signals, reducing system design costs. 8bit D/A converter can be used for audio playback or power control. The temperature sensor integrated in the chip can realize real-time monitoring of the external ambient temperature. The internally integrated comparator of the chip can support both high-speed and low-speed operating modes. In the high-speed mode, it can support the control feedback of the high-speed motor, and in the low-speed mode, it can be used for battery monitoring. Integrate a variety of advanced timer modules, load 1-channel SysTick timer, 17-channel 16bit timer, 1-channel 15bit interval timer, watchdog timer and real-time clock and other functions, and can support general-purpose PWM and motor-specific PWM applications.

BAT32G179 also has excellent low-power performance, supports two low-power modes of sleep and deep sleep, and is designed to be flexible. Its operating power consumption is 120uA/MHz@64MHz, and the power consumption is only 1.5uA in deep sleep mode, which is suitable for battery-powered low-power devices. At the same time, due to the integrated event linkage controller, direct connection between hardware modules can be realized without the intervention of the CPU, which is faster than using interrupt response, while reducing the frequency of CPU activity and prolonging the battery life.

These features make the BAT32G179 microcontroller series widely applicable to energy storage, battery packs, motor control, security, power, and other applications.

1.2 Product Model List



List of products of BAT32G179:

Number of Pin	Encapsulation	Product model
64-pin	64-pin plastic package LQFP (7×7mm, 0.4mm pitch)	BAT32G179GM64FB
80-pin	80-pin plastic package LQFP (12×12mm, 0.5mm pitch)	BAT32G179GM80FA
100-pin	100-pin plastic package LQFP (14×14mm, 0.5mm pitch)	BAT32G179GM100FA

FLASH, SRAM capacity:

Flash memory	Special data Flash memory	SRAM	BAT32G179		
			64-pin	80-pin	100-pin
512KB	20KB	64KB	BAT32G179GM64	BAT32G179GM80	BAT32G179GM100

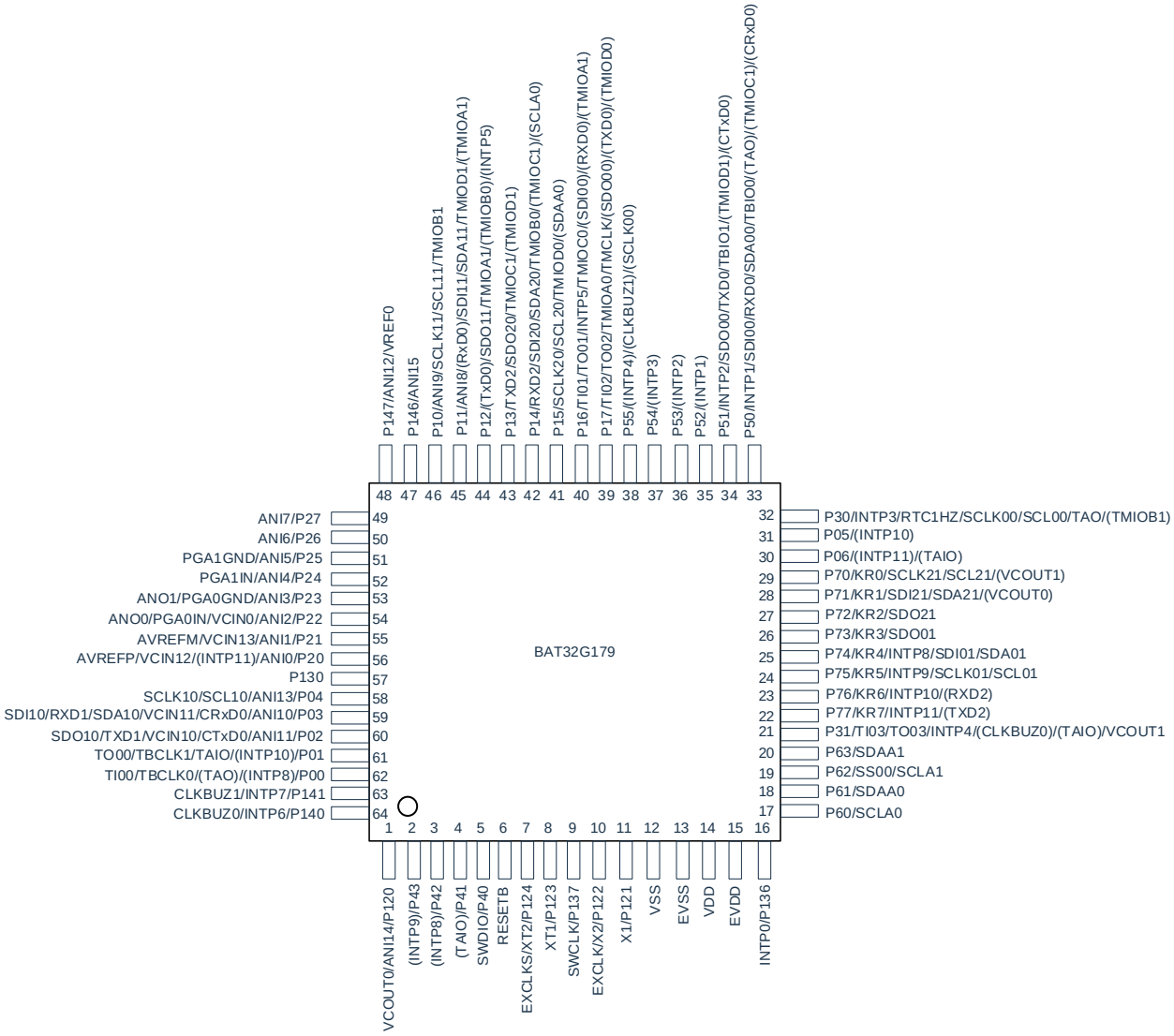
Product selection table of BAT32G179:

Part No.	Kernel	Dominant frequency (MHz)	Min operating voltage (V)	Maxoperating voltage (V)	Code Flash (kB)	SRAM (KB)	Data Flash (KB)	DMA	GPIO	12bit ADC	8bit DAC	Comparator CMP	Amplifier PGA	Universal timer (16bit)	Real time clock (RTC)	Watchdog timer (WDT)	Asynchronous serial bus	Synchronous serial bus	IIC bus	LIN bus	CAN bus	Hardware multiplier	Hardware diyider	package
BAT32G179 GM64FB	M0+	64	1.8	5.5	512	64	20	37	59	16+4	2	2	2	17	1	1	3	6	2+6	1	1	Y	Y	LQFP 64
BAT32G179 GM80FA	M0+	64	1.8	5.5	512	64	20	38	75	22+4	2	2	2	17	1	1	4	1+8	2+8	1	2	Y	Y	LQFP 80
BAT32G179 GM100FA	M0+	64	1.8	5.5	512	64	20	40	93	28+4	2	2	2	17	1	1	4	2+8	2+8	1	3	Y	Y	LQFP 100

1.3 Pin connection diagram (Top View)

1.3.1 BAT32G179GM64FB

- 64-pin plastic package LQFP(7x7mm, 0.4mm pitch)

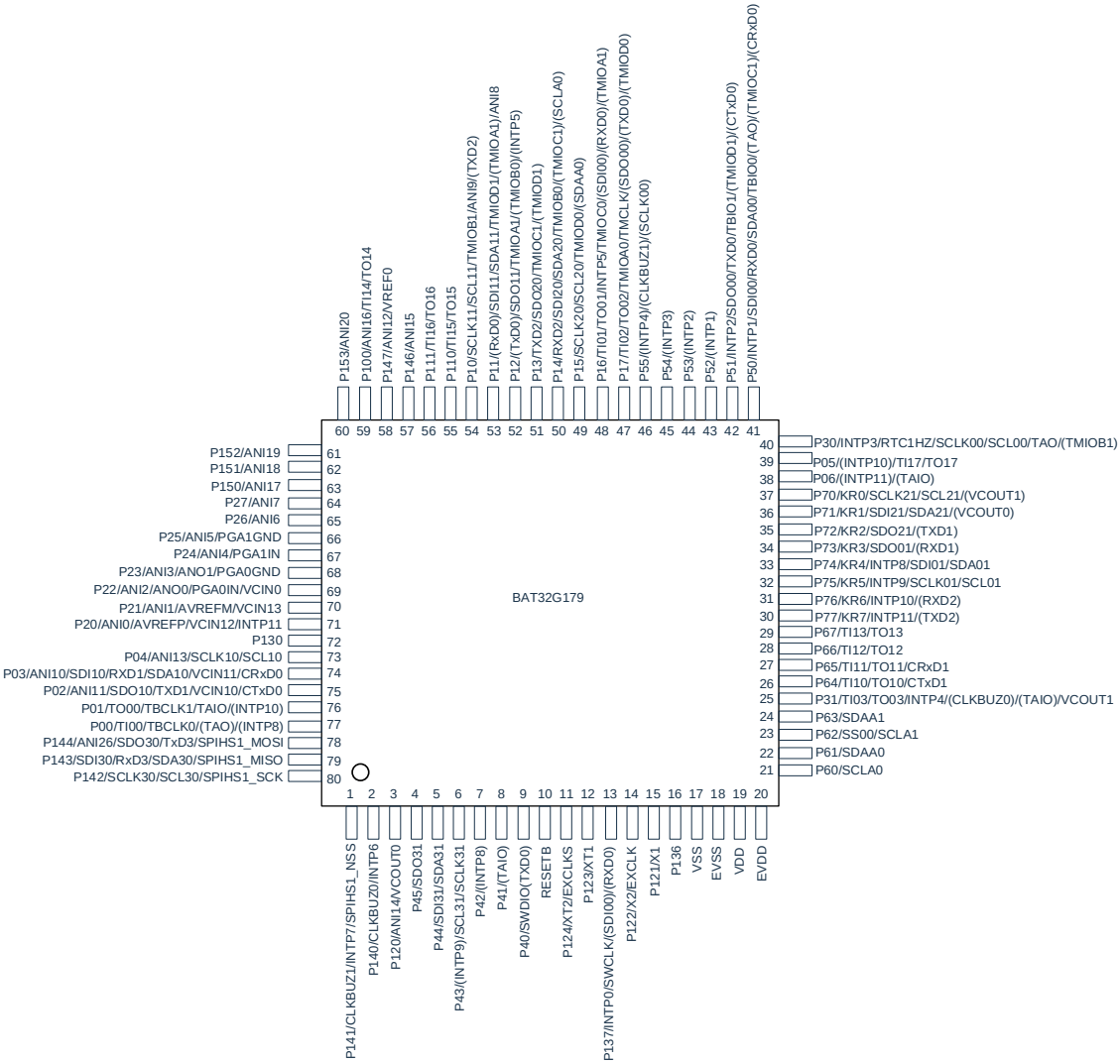


Note:

1. EV_{SS} pin and V_{SS} pin must be at the same potential
2. The voltage of V_{DD} pin must be equal to the voltage of EV_{DD} pin.
3. When using the microcontroller for an application where the noise generated inside the microcontroller must be reduced, it is recommended to supply separate powers to the V_{DD} and EV_{DD} pins and connect the V_{SS} and EV_{SS} pins to separateground lines.
4. Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register.

1.3.2 BAT32G179GM80FA

- 80-pin plastic package LQFP(12x12mm, 0.5mm pitch)

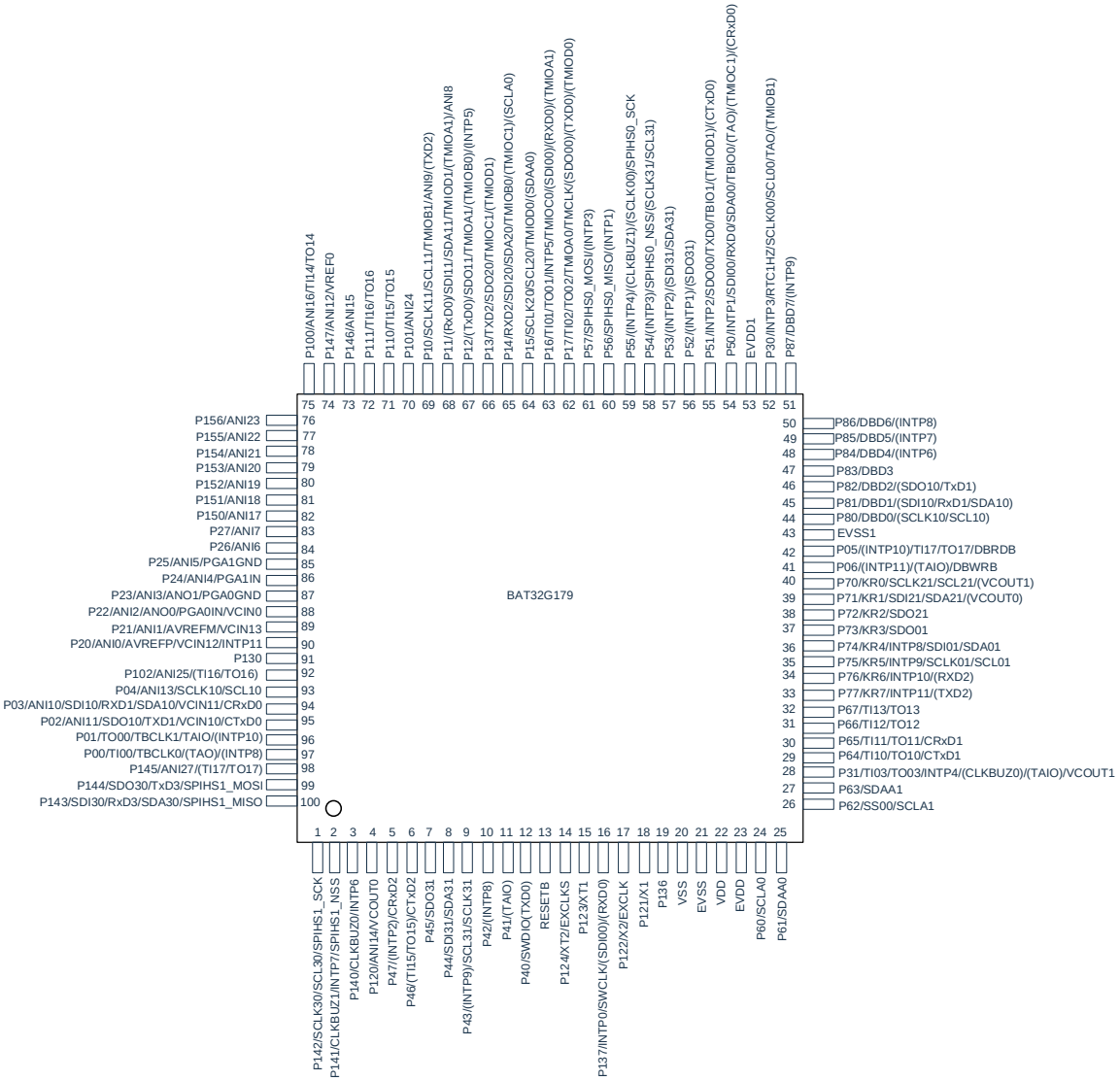


Note:

1. EV_{SS} pin and V_{SS} pin must be at the same potential
2. The voltage of V_{DD} pin must be equal to the voltage of EV_{DD} pin.
3. When using the microcontroller for an application where the noise generated inside the microcontroller must be reduced, it is recommended to supply separate powers to the V_{DD} and EV_{DD} pins and connect the V_{SS} and EV_{SS} pins to separateground lines.
4. Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register.

1.3.3 BAT32G179GM100FA

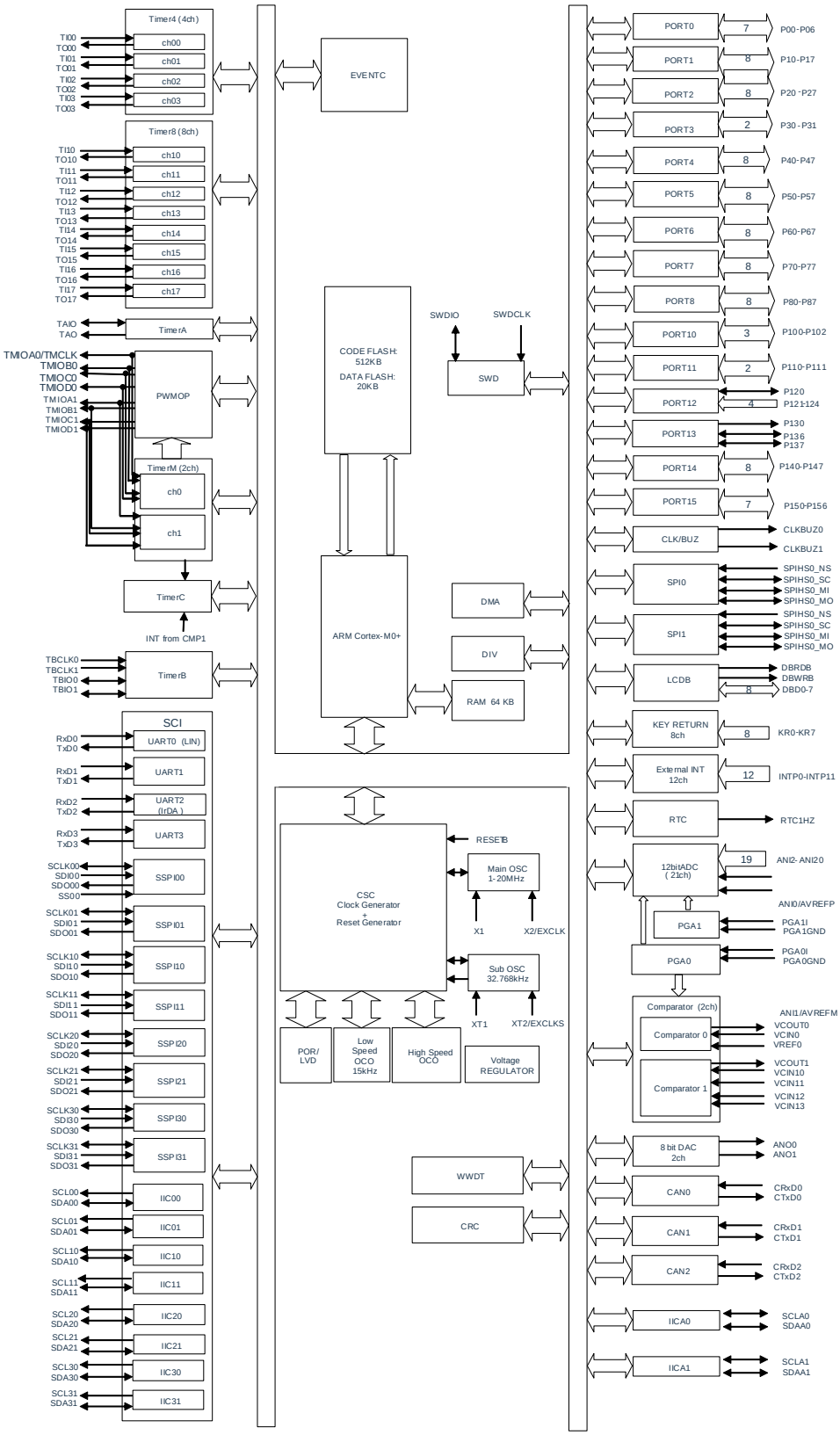
- 100-pin plastic package LQFP(14x14mm, 0.5mm pitch)



Note:

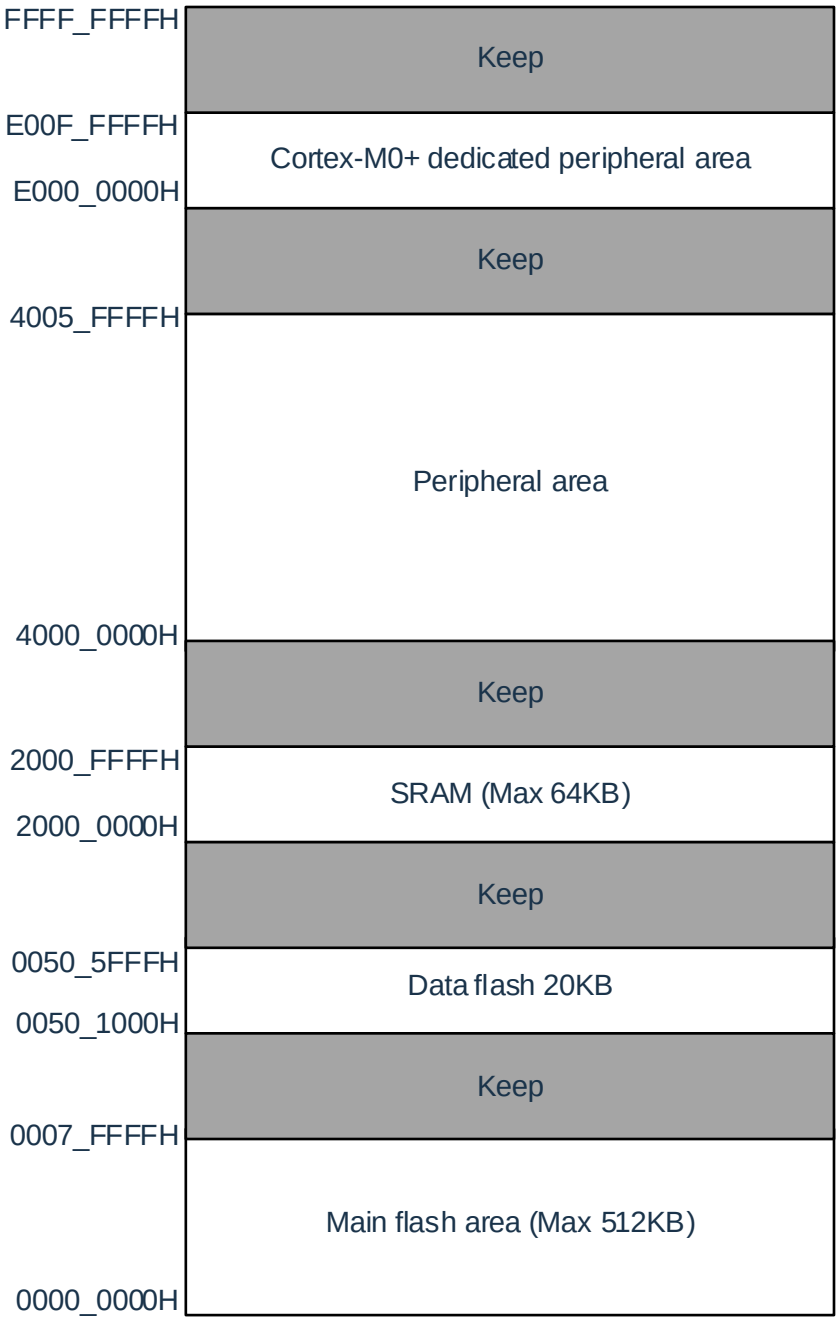
1. EV_{SS} pin and V_{SS} pin must be at the same potential
2. The voltage of V_{DD} pin must be equal to the voltage of EV_{DD} pin.
3. When using the microcontroller for an application where the noise generated inside the microcontroller must be reduced, it is recommended to supply separate powers to the V_{DD} and EV_{DD} pins and connect the V_{SS} and EV_{SS} pins to separategroundlines.
4. Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register.

2 Block Diagram



Note: The above is for 100-pin product. Some functions of products below 100-pin are not supported.

3 Memory Mapping



4 Pin Function

4.1 Port Function

The relationship between power supply and pins is as follows

Power/ground	Corresponding Pin
EVDD/EVSS	• Port pins other than P20~P27, P121~P124, P137 and RESETB
VDD/VSS	• P20~P27, P121~P124, P137 and RESETB

4.1.1 64-pin Products

(1/2)

Function Name	I/O	After Reset Release	Alternate Function	Function
P00	I/ O	Input port	TI00/TBCLK0/(TAO)/(INTP8)	Port 0. 7-bit I/O port. Input/output can be specified in 1-bit units. Use of an on-chip pull-up resistor can be specified by a software setting at input port. Input of P01, P03 and P04 can be set to TTL input buffer. Output of P00 can be set to N-ch open-drain output (V_{DD} tolerance). P00 and P02 to P04 can be set to analog input
P01			TO00/TBCLK1/TAIO/(INTP10)	
P02		Analog function	ANI11/SDO10/TXD1/VCIN10/CTxD0	
P03			ANI10/SDI10/RXD1/SDA10/VCIN11/CRxD0	
P04			ANI13/SCLK10/SCL10	
P05		Input port	(INTP10)	
P06			(INTP11)/(TAIO)	
P10	I/ O	Analog function	SCLK11/SCL11/TMIOB1/ANI9	Port 1. 8-bit I/O port. Input/output can be specified in 1-bit units. Use of an on-chip pull-up resistor can be specified by a software setting at input port. Input of P10 and P14 to P17 can be set to TTL input buffer. Output of P10, P11, P13 to P15, and P17 can be set to N-ch open-drain output (V_{DD} tolerance). P10 to P11 can be set to analog input.
P11			(RxD0)/SDI11/SDA11/TMIOD1/(TMIOA1)/ANI8	
P12		Input port	(TxD0)/SDO11/TMIOA1/(TMIOB0)/(INTP5)	
P13			TXD2/SDO20/TMIOC1/(TMIOD1)	
P14			RXD2/SDI20/SDA20/TMIOB0/(TMIOC1)/(SCLA0)	
P15			SCLK20/SCL20/TMIOD0/(SDAA0)	
P16			TI01/TO01/INTP5/TMIOC0/(SDI00)/(RXD0)/(TMIOA1)	
P17			TI02/TO02/TMIOA0/TMCLK/(SDO00)/(TXD0)/(TMIOD0)	
P20	I/ O	Analog function	ANI0/AVREFP/VCIN12/(INTP11)	Port 2. 8-bit I/O port. Input/output can be specified in 1-bit units. Can be set to analog input.
P21			ANI1/AVREFM/VCIN13	
P22			ANI2/ANO0/PGA0IN/VCIN0	
P23			ANI3/ANO1/PGA0GND	
P24			ANI4/PGA1IN	
P25			ANI5/PGA1GND	
P26			ANI6	
P27			ANI7	
P30	I/ O	Input port	INTP3/RTC1HZ/SCLK00/SCL00/TAO/(TMIOB1)	Port 3. 2-bit I/O port. Input/output can be specified in 1-bit units. Use of an on-chip pull-up resistor can be specified by a software setting at input port. Input of P30 can be set to TTL input buffer. Output of P30 can be set to N-ch Open-drain output (V_{DD} tolerance).
P31			TI03/TO03/INTP4/(CLKBUZ0)/(TAIO)/VCOUT1	

(2/2)

Function Name	I/O	After Reset Release	Alternate Function	Function
P40	I/ O	Input port	SWDIO	Port 4. 4-bit I/O port. Input/output can be specified in 1-bit units. Use of an on-chip pull-up resistor can be specified by a software setting at input port.
P41			(TAIO)	
P42			(INTP8)	
P43			(INTP9)	
P50	I/ O	Input port	INTP1/SDI00/RXD0/SDA00/TBIO0/(TAO)/(TMIOC1)/(CRxD0)	Port 5. 6-bit I/O port. Input/output can be specified in 1-bit units. Use of an on-chip pull-up resistor can be specified by a software setting at input port. Input of P50 andP51 can be set to TTL input buffer. Output of P50, p51 and P55 can be set to N-ch opendrain output (V_{DD} tolerance).
P51			INTP2/SDO00/TXD0/TBIO1/(TMIOD1)/(CTxD0)	
P52			(INTP1)	
P53			(INTP2)	
P54			(INTP3)	
P55			(INTP4)/(CLKBUZ1)/(SCLK00)	
P60	I/ O	Input port	SCLA0	Port 6 4-bit I/O port. Input/output can be specified in 1-bit units. Output of P60~ P63 can be set to N-ch opendrain output (6V tolerance).
P61			SDAA0	
P62			SS00/SCLA1	
P63			SDAA1	
P70	I/ O	Input port	KR0/SCLK21/SCL21/(VCOUT1)	Port 7. 8-bit I/O port. Input/output can be specified in 1-bit units. Use of an on-chip pull-up resistor can be specified by a software setting at input port. Output of P71 and P74 can be set to N-ch opendrain output (EV_{DD} tolerance).
P71			KR1/SDI21/SDA21/(VCOUT0)	
P72			KR2/SDO21	
P73			KR3/SDO01	
P74			KR4/INTP8/SDI01/SDA01	
P75			KR5/INTP9/SCLK01/SCL01	
P76			KR6/INTP10/(RxD2)	
P77			KR7/INTP11/(TxD2)	
P120	I/ O	Analog function	ANI14/VCOUT0	Port 12. 1-bit I/O port and 2-bit input-only port. For only P120, input/output can be specified. For only P120, use of an on-chip pull-up resistor can be specified by a software setting at input port. P120 can be set to analog input.
P121	I	Input port	X1	
P122			X2/EXCLK	
P123			XT1	
P124			XT2/EXCLKS	
P130	O	Output port	—	Port 13. 1-bit I/O port and 2-bit input-only port. P136 and P137 can be designated as input or output in bit units. The input port can be set by software, using internal pull-up resistors.
P136	I/ O	Input port	INTP0	
P137			SWCLK	
P140	I/ O	Input port	CLKBUZ0/INTP6	Port 14. 4-bit I/O port. Input/output can be specified. Use of an on-chip pull-up resistor can be specified by a software setting at input port.
P141			CLKBUZ1/INTP7	
P146		Analog function	ANI15	
P147			ANI12/VREF0	

				P146 and P147 can be set as analog input.
RESETB	I	—	—	Input-only pin for external reset. Connect to V_{DD} directly or via a resistor when external reset is not used.。

Note:

1. Each pin can be specified as either digital or analog by setting port mode control register x (PMCx) (Can be specified in 1-bit units).
2. Description of Alternate function,please refer to “4.2 Port Multiplexing Function”.
3. Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register.

4.1.2 80-pin Products

(1/2)

Function Name	I/O	After Reset Release	Alternate Function	Function
P00	I/ O	Input port	TI00/TBCLK0/(TAO)/(INTP8)	Port 0. 7-bit I/O port. Input/output can be specified in 1-bit units. Use of an on-chip pull-up resistor can be specified by a software setting at input port. Input of P01, P03 and P04 can be set to TTL input buffer. Output of P00, P02 to P04 can be set to N-ch open-drain output (EV_{DD} tolerance). P02, P03 and P04 can be set to analog input
P01			TO00/TBCLK1/TAIO/(INTP10)	
P02		Analog function	ANI11/SDO10/TXD1/VCIN10/CTxD0	
P03			ANI10/SDI10/RXD1/SDA10/VCIN11/CRxD0	
P04			ANI13/SCLK10/SCL10	
P05		Input port	(INTP10)/TI17/TO17	
P06			(INTP11)/(TAIO)	
P10	I/ O	Analog function	SCLK11/SCL11/TMIOB1/ANI9/(TXD2)	Port 1. 8-bit I/O port. Input/output can be specified in 1-bit units. Use of an on-chip pull-up resistor can be specified by a software setting at input port. Input of P10 and P14 to P17 can be set to TTL input buffer. Output of P10, P11, P13 to P15, and P17 can be set to N-ch open-drain output (EV_{DD} tolerance). P10 and P11 can be set to analog input.
P11			(RxD0)/SDI11/SDA11/TMIOD1/(TMIOA1)/ANI8	
P12		Input port	(TxD0)/SDO11/TMIOA1/(TMIOB0)/(INTP5)	
P13			TXD2/SDO20/TMIOC1/(TMIOD1)	
P14			RXD2/SDI20/SDA20/TMIOB0/(TMIOC1)/(SCLA0)	
P15			SCLK20/SCL20/TMIOD0/(SDAA0)	
P16			TI01/TO01/INTP5/TMIOC0/(SDI00)/(RXD0)/(TMIOA1)	
P17			TI02/TO02/TMIOA0/TMCLK/(SDO00)/(TXD0)/(TMIOD0)	
P20	I/ O	Analog function	ANI0/AVREFP/VCIN12/(INTP11)	Port 2. 8-bit I/O port. Input/output can be specified in 1-bit units. Can be set to analog input.
P21			ANI1/AVREFM/VCIN13	
P22			ANI2/ANO0/PGA0IN/VCIN0	
P23			ANI3/ANO1/PGA0GND	
P24			ANI4/PGA1IN	
P25			ANI5/PGA1GND	
P26			ANI6	
P27			ANI7	
P30	I/ O	Input port	INTP3/RTC1HZ/SCLK00/SCL00/TAO/(TMIOB1)	Port 3. 2-bit I/O port. Input/output can be specified in 1-bit units. Use of an on-chip pull-up resistor can be specified by a software setting at input port. Input of P30 can be set to TTL input buffer. Output of P30 can be set to N-ch Open-drain output (EV_{DD} tolerance).
P31			TI03/TO03/INTP4/(CLKBUZ0)/(TAIO)/VCOUT1	

(2/2)

Function Name	I/O	After Reset Release	Alternate Function	Function
P40	I/ O	Input port	SWDIO	Port 4 6-bit I/O port. Input/output can be specified in 1-bit units. Use of an on-chip pull-up resistor can be specified by a software setting at input port. Input of P43 and P44 can be set to TTL input buffer. Output of P43 and P44 can be set to N-ch Open-drain output (EV_{DD} tolerance).
P41			(TAIO)	
P42			(INTP8)	
P43			(INTP9)/SCLK31/SCL31	
P44			SDA31/SDI31	
P45			SDO31	
P50	I/ O	Input port	INTP1/SDI00/RXD0/SDA00/TBIO0/(TAO)/(TMIOC1)/(CRxD0)	Port 5 6-bit I/O port. Input/output can be specified in 1-bit units. Use of an on-chip pull-up resistor can be specified by a software setting at input port. Input of P50 and P55 can be set to TTL input buffer. Output of P50, P51 and P55 can be set to N-ch Open-drain output (EV_{DD} tolerance).
P51			INTP2/SDO00/TXD0/TBIO1/(TMIOD1)/(CTxD0)	
P52			(INTP1)	
P53			(INTP2)	
P54			(INTP3)	
P55			(INTP4)/(CLKBUZ1)/(SCLK00)	
P60	I/ O	Input port	SCLA0	Port 6 8-bit I/O port. Input/output can be specified in 1-bit units. Output of P60 to P63 can be set to N-ch Open-drain output (6V tolerance).
P61			SDAA0	
P62			SS00/SCLA1	
P63			SDAA1	
P64			TI10/TO10/CTxD1	
P65			TI11/TO11/CRxD1	
P66			TI12/TO12	
P67			TI13/TO13	
P70	I/ O	Input port	KR0/SCLK21/SCL21/(VCOUT1)	Port 7. 8-bit I/O port. Input/output can be specified in 1-bit units. Use of an on-chip pull-up resistor can be specified by a software setting at input port. Output of P71 and P74 can be set to N-ch open-drain output (EV_{DD} tolerance).
P71			KR1/SDI21/SDA21/(VCOUT0)	
P72			KR2/SDO21/(TXD1)	
P73			KR3/SDO01/(RXD1)	
P74			KR4/INTP8/SDI01/SDA01	
P75			KR5/INTP9/SCLK01/SCL01	
P76			KR6/INTP10/(RxD2)	
P77			KR7/INTP11/(TxD2)	
P100	I/ O	Analog function	ANI16/TI14/TO14	Port 10. 1-bit I/O port. Input/output can be specified in 1-bit units. Use of an on-chip pull-up resistor can be specified by a software setting at input port.
P110	I/ O	Input port	TI15/TO15	Port 11. 2-bit I/O port. Input/output can be specified in 1-bit units. Use of an on-chip pull-up resistor can be specified by a software setting at input port.
P111			TI16/TO16	
P120	I/ O	Analog function	ANI14/VCOUT0	Port 12. 1-bit I/O port and 2-bit input-only port. For only P120, input/output can be specified. For only P120, use of an on-chip pull-up resistor can be specified by a software setting at input port. P120 can be set to analog input.
P121	I	Input port	X1	
P122			X2/EXCLK	
P123			XT1	
P124			XT2/EXCLKS	
P130	O	Output port	—	Port 13. 1-bit I/O port and 2-bit input-only port. P136 and P137 can be designated as input or output in bit units. The input port can be set by
P136	I/ O	Input port	—	
P137			INTP0/SWCLK/(SDI00)/(RXD0)	

				software, using internal pull-up resistors.
P140	I/ O	Input port	CLKBUZ0/INTP6	Port 14. 7-bit I/O port. Input/output can be specified in 1-bit units. Use of an on-chip pull-up resistor can be specified by a software setting at input port. Input of P142 and P143 can be set to TTL input buffer. Output of P142, P143, and P144 can be set to N-ch open-drain output (EV_{DD} tolerance). P144, P146 and P147 can be set to analog input
P141			CLKBUZ1/INTP7/SPIHS1_NSS	
P142			SCLK30/SCL30/SPIHS1_SCK	
P143			SDI30/RxD3/SDA30/SPIHS1_SCK	
P144			ANI26/SDO30/TxD3/SPIHS1_MOSI	
P146		Analog function	ANI15	
P147			ANI12/VREF0	
P150	I/ O	Analog function	ANI17	Port 15. 4-bit I/O port. Input/output can be specified in 1-bit units. Use of an on-chip pull-up resistor can be specified by a software setting at input port. Can be set to analog input
P151			ANI18	
P152			ANI19	
P153			ANI20	
RESETB	I	—	—	Input-only pin for external reset. Connect to V_{DD} directly or via a resistor when external reset is not used.

Note:

1. Each pin can be specified as either digital or analog by setting port mode control register x (PMCx) (Can be specified in 1-bit units).
2. Description of Alternate function,please refer to “4.2 Port Multiplexing Function”.
3. Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register.

4.1.3 100-pin Products

（1/3）

Function Name	I/O	After Reset Release	Alternate Function	Function
P00	I/ O	Input port	TI00/TBCLK0/(TAO)/(INTP8)	Port 0. 7-bit I/O port. Input/output can be specified in 1-bit units. Use of an on-chip pull-up resistor can be specified by a software setting at input port. Input of P01, P03 and P04 can be set to TTL input buffer. Output of P00 can be set to N-ch open-drain output (V_{DD} tolerance). P00 and P02 to P04 can be set to analog input
P01			TO00/TBCLK1/TAIO/(INTP10)	
P02		Analog function	ANI11/SDO10/TXD1/VCIN10/CTxD0	
P03			ANI10/SDI10/RXD1/SDA10/VCIN11/CRxD0	
P04			ANI13/SCLK10/SCL10	
P05		Input port	(INTP10)/TI17/TO17/DBRDB	
P06			(INTP11)/(TAIO)/DBWRB	
P10	I/ O	Analog function	SCLK11/SCL11/TMIOB1/ANI9/(TXD2)	Port 1. 8-bit I/O port. Input/output can be specified in 1-bit units. Use of an on-chip pull-up resistor can be specified by a software setting at input port. Input of P10 and P14 to P17 can be set to TTL input buffer. Output of P10, P11, P13 to P15, and P17 can be set to N-ch open-drain output (V_{DD} tolerance). P10 to P11 can be set to analog input.
P11			(RxD0)/SDI11/SDA11/TMIOD1/(TMIOA1)/ANI8	
P12		Input port	(TxD0)/SDO11/TMIOA1/(TMIOB0)/(INTP5)	
P13			TXD2/SDO20/TMIOC1/(TMIOD1)	
P14			RXD2/SDI20/SDA20/TMIOB0/(TMIOC1)/(SCLA0)	
P15			SCLK20/SCL20/TMIOD0/(SDAA0)	
P16			TI01/TO01/INTP5/TMIOC0/(SDI00)/(RXD0)/(TMIOA1)	
P17			TI02/TO02/TMIOA0/TMCLK/(SDO00)/(TXD0)/(TMIOD0)	
P20	I/ O	Analog function	ANI0/AVREFP/VCIN12/INTP11	Port 2. 8-bit I/O port. Input/output can be specified in 1-bit units. Can be set to analog input.
P21			ANI1/AVREFM/VCIN13	
P22			ANI2/ANO0/PGA0IN/VCIN0	
P23			ANI3/ANO1/PGA0GND	
P24			ANI4/PGA1IN	
P25			ANI5/PGA1GND	
P26			ANI6	
P27			ANI7	
P30	I/ O	Input port	INTP3/RTC1HZ/SCLK00/SCL00/TAO/(TMIOB1)	Port 3. 2-bit I/O port. Input/output can be specified in 1-bit units. Use of an on-chip pull-up resistor can be specified by a software setting at input port. Input of P30 can be set to TTL input buffer. Output of P30 can be set to N-ch Open-drain output (V_{DD} tolerance).
P31			TI03/TO03/INTP4/(CLKBUZ0)/(TAIO)/VCOUT1	

（2/3）

Function Name	I/O	After Reset Release	Alternate Function	Function
P40	I/ O	Input port	SWDIO	Port 4. 8-bit I/O port. Input/output can be specified in 1-bit units. Use of an on-chip pull-up resistor can be specified by a software setting at input port. Input of P43 and P44 can be set to TTL input buffer. and the output can be set to N-ch opendrain output (EV_{DD} tolerance).
P41			(TAIO)	
P42			(INTP8)	
P43			(INTP9)/SCLK31/SCL31	
P44			SDA31/SDI31	
P45			SDO31	
P46			CTxD2/(TI15/TO15)	
P47			CRxD2/(INTP2)	
P50	I/ O	Input port	INTP1/SDI00/RXD0/SDA00/TBIO0/(TAO)/(TMIOC1)/(CRxD0)	Port 5. 6-bit I/O port. Input/output can be specified in 1-bit units. Use of an on-chip pull-up resistor can be specified by a software setting at input port. Input of P50 andP51 can be set to TTL input buffer. Output of P50, p51 and P55 can be set to N-ch opendrain output (V_{DD} tolerance).
P51			INTP2/SDO00/TXD0/TBIO1/(TMIOD1)/(CTxD0)	
P52			(INTP1)/(SDO31)	
P53			(INTP2)/(SDI31/SDA31)	
P54			(INTP3)/(SCLK31/SCL31)/SPIHS0_NSS	
P55			(INTP4)/(CLKBUZ1)/(SCLK00)/SPIHS0_SCK	
P56			SPIHS0_MISO/(INTP1)	
P57			SPIHS0_MOSI/(INTP3)	
P60	I/ O	Input port	SCLA0	Port 6 8-bit I/O port. Input/output can be specified in 1-bit units. Output of P60~ P63 can be set to N-ch opendrain output (6V tolerance).
P61			SDAA0	
P62			SS00/SCLA1	
P63			SDAA1	
P64			TI10/TO10/CTxD1	
P65			TI11/TO11/CRxD1	
P66			TI12/TO12	
P67			TI13/TO13	
P70	I/ O	Input port	KR0/SCLK21/SCL21/(VCOUT1)	Port 7. 8-bit I/O port. Input/output can be specified in 1-bit units. Use of an on-chip pull-up resistor can be specified by a software setting at input port. Output of P71 and P74 can be set to N-ch opendrain output (EV_{DD} tolerance).
P71			KR1/SDI21/SDA21/(VCOUT0)	
P72			KR2/SDO21	
P73			KR3/SDO01	
P74			KR4/INTP8/SDI01/SDA01	
P75			KR5/INTP9/SCLK01/SCL01	
P76			KR6/INTP10/(RxD2)	
P77			KR7/INTP11/(TxD2)	

（3/3）

Function Name	I/O	After Reset Release	Alternate Function	Function
P80	I/ O	Input port	(SCLK10/SCL10)/DBD0	Port 8 8-bit I/O port. Input/output can be specified in 1-bit units. Use of an on-chip pull-up resistor can be specified by a software setting at input port. Input of P80 and P81 can be set to TTL input buffer. Output of P80, P81 and P82 can be set to N-ch Open-drain output (EV_{DD} tolerance).
P81			(SDI10/RXD1/SDA10)/DBD1	
P82			(SDO10/TXD1)/DBD2	
P83			DBD3	
P84			(INTP6)/DBD4	
P85			(INTP7)/DBD5	
P86			(INTP8)/DBD6	
P87			(INTP9)/DBD7	
P100	I/ O	Analog function	ANI16/TI14/TO14	Port 10. 3-bit I/O port. Input/output can be specified in 1-bit units. Use of an on-chip pull-up resistor can be specified by a software setting at input port.
P101			ANI24	
P102			(TI16/TO16)/ANI25	
P110	I/ O	Input port	TI15/TO15	Port 11. 2-bit I/O port. Input/output can be specified in 1-bit units. Use of an on-chip pull-up resistor can be specified by a software setting at input port.
P111			TI16/TO16	
P120	I/ O	Analog function	ANI14/VCOUT0	Port 12. 1-bit I/O port and 2-bit input-only port. For only P120, input/output can be specified. For only P120, use of an on-chip pull-up resistor can be specified by a software setting at input port. P120 can be set to analog input.
P121	I	Input port	X1	
P122			X2/EXCLK	
P123			XT1	
P124			XT2/EXCLKS	
P130	O	Output port	—	Port 13. 1-bit I/O port and 2-bit input-only port. P136 and P137 can be designated as input or output in bit units. The input port can be set by software, using internal pull-up resistors.
P136	I/ O	Input port	—	
P137			INTP0/SWCLK/(SDI00)/(RXD0)	
P140	I/ O	Input port	CLKBUZ0/INTP6	Port 14. 7-bit I/O port. Input/output can be specified in 1-bit units. Use of an on-chip pull-up resistor can be specified by a software setting at input port. Input of P142 and P143 can be set to TTL input buffer. Output of P142, P143, and P144 can be set to N-ch open-drain output (EV_{DD} tolerance). P144, P145, P146 and P147 can be set to analog input
P141			CLKBUZ1/INTP7/SPIHS1_NSS	
P142			SCLK30/SCL30/SPIHS1_SCK	
P143			SDI30/RxD3/SDA30/SPIHS1_MISO	
P144			ANI26/SDO30/TxD3/SPIHS1_MOSI	
P145		Analog function	(TI17/TO17)/ANI27	
P146			ANI15	
P147			ANI12/VREF0	
P150	I/ O	Analog function	ANI17	Port 15. 4-bit I/O port. Input/output can be specified in 1-bit units. Use of an on-chip pull-up resistor can be specified by a software setting at input port. Can be set to analog input
P151			ANI18	
P152			ANI19	
P153			ANI20	
P154			ANI21	
P155			ANI22	
P156			ANI23	
RESETB	I	—	—	Input-only pin for external reset. Connect to VDD directly or via a resistor

				when external reset is not used.

Note:

1. Each pin can be specified as either digital or analog by setting port mode control register x (PMCx) (Can be specified in 1-bit units).
2. Description of Alternate function,please refer to “4.2 Port Multiplexing Function”.
3. Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register.

4.2 Port Multiplexing Function

（1/2）

Function Name	Input/Output	Function
ANI0~ANI27	input	Analog input of A/D converter
ANO0, ANO1	output	D/A converter output
INTP0~INTP11	input	External interrupt request input Designation of valid edges: rising edge, falling edge, rising and falling double edges
VCIN0	input	Analog voltage input of comparator 0
VCIN10, VCIN11, VCIN12, VCIN13	input	Comparator1's analog voltage/reference voltage input
VREF0	input	Reference voltage input of comparator0
VCOUT0, VCOUT1	output	Comparator output
PGA0IN，PGA1IN	input	PGA input
PGA0GND，PGA1GND	input	PGA reference input
KR0~KR7	input	Key interrupt input
CLKBUZ0, CLKBUZ1	output	Clock output / buzzer output
RTC1HZ	output	Real-time clock correction clock (1Hz) output
RESETB	input	Low-level active system reset input. When external reset is not used, it must be connected to V_{DD} directly or through a resistor.
CRxD0,CRxD1,CRxD2	input	CAN serial data input
CTxD0,CTxD1,CTxD2	output	CAN serial data output
RxD0~RxD3	input	Serial interface UART0, UART1, UART2 serial data input
TxD0~TxD3	output	Serial interface UART0, UART1, UART2 serial data output
SCL00, SCL01, SCL10, SCL11, SCL20, SCL21, SCL30, SCL31	output	Serial interface IIC00, IIC01, IIC10, IIC11, IIC20, IIC21, IIC30, IIC31 serial clock output
SDA00, SDA01, SDA10, SDA11, SDA20, SDA21, SDA30, SDA31	input / output	Serial interface IIC00, IIC01, IIC10, IIC11, IIC20, IIC21, IIC30, IIC31 serial clock input/ output
SCLK00, SCLK01, SCLK10, SCLK11, SCLK20, SCLK21, SCLK30, SCLK31	input / output	Serial interface SSPI00, SSPI01, SSPI10, SSPI11, SSPI20, SSPI21, SSPI30, SSPI31 serial clock input/ output
SDI00, SDI01, SDI10, SDI11, SDI20, SDI21, SDI30, SDI31	input	Serial interface SSPI00, SSPI01, SSPI10, SSPI11, SSPI20, SSPI21, SSPI30, SSPI31 serial clock input/ output
SS00	input	Chip select input of serial interface SSPI00t
SDO00, SDO01, SDO10, SDO11, SDO20, SDO21, SDO30, SDO31	output	Serial data output of SSPI00, SSPI01, SSPI10, SSPI11, SSPI20, SSPI21, SSPI30, SSPI31
DBD0~DBD7	input / output	LCD bus data input/output
DBRDB	output	LCD bus read enable output
DBWRB	output	LCD bus write enable output
SCLA0, SCLA1	input / output	Serial interface IICA0, IICA1 clock input/output
SDAA0, SDAA1	input / output	Serial interface IICA0, IICA1 serial data input/output

（2/2）

Function Name	Input / Output	Function
SPIHS0_NSS	input	Chip select input of serial interface SPIHS0
SPIHS0_SCK	input / output	Serial clock input/output of serial interface SPIHS0
SPIHS0_MISO	input / output	Serial data input/output of serial interface SPIHS0
SPIHS0_MOSI	input / output	Serial data input/output of serial interface SPIHS0
SPIHS1_NSS	input	Chip select input of serial interface SPIHS1
SPIHS1_SCK	input / output	Serial clock input/output of serial interface SPIHS1
SPIHS1_MISO	input / output	Serial data input/output of serial interface SPIHS1
SPIHS1_MOSI	input / output	Serial data input/output of serial interface SPIHS1
TI00~TI03	input	16-bit timer Timer4 external count clock/capture trigger input
TO00~TO03	output	Timer output of 16-bit timer Timer4
TI10~TI17	input	16-bit timer Timer8 external count clock/capture trigger input
TO10~TO17	output	Timer output of 16-bit timer Timer8
TAIO	input / output	Timer TimerA input/output
TAO	output	Timer TimerA output
TMCLK	input	Timer TimerM external clock input
TMIOA0, TMIOB0, TMIOC0, TMIOD0, TMIOA1, TMIOB1, TMIOC1, TMIOD1	input / output	Timer TimerM input/output
TBIO0, TBIO1	input / output	Timer TimerB input/output
TBCLK0, TBCLK1	input	Timer TimerB external clock input
X1, X2	—	Connect the resonator for the main system clock.
EXCLK	input	External clock input of main system clock
XT1, XT2	—	Connect the resonator for the subsystem clock.
EXCLKS	input	External clock input for subsystem clock
V_{DD}	—	＜64, 80 pin product＞: Power supply for P20~P27, P121~P124, P137 and RESETB pins
EV_{DD}	—	Power supply for port pins (except P20~P27, P121~P124, P137 and RESETB)
AVREFP	input	Positive (+) reference voltage input of A/D converter
AVREFM	input	Negative (-) reference voltage input of A/D converter
V_{SS}	—	＜64, 80 pin product＞: Ground potential of P20~P27, P121~P124, P137 and RESETB pin
EV_{SS}	—	Ground potential of port pins (except P20~P27, P121~P124, P137 and RESETB)
SWDIO	input / output	SWD data interface
SWCLK	input	SWD clock interface

Remark: As a countermeasure for noise and locking, the bypass capacitor (about 0.1uF) must be connected with the shortest distance between V_{DD}-V_{SS} and EV_{DD}-EV_{SS} and thicker wiring.

5 Function Summary

5.1 ARM® Cortex®-M0+ Core

ARM's Cortex-M0+ processor is a new generation of ARM processors for embedded systems. It provides a low-cost platform designed to meet the needs of a small pin count and low-power microcontroller, while providing excellent computing performance and advanced system response to interrupts.

The 32-bit RISC processor of the Cortex-M0+ processor provides excellent code efficiency and the expected high performance of the ARM core, which is different from 8-bit and 16-bit devices of the same memory size. The Cortex-M0+ processor has 32 address lines and a storage space of up to 4G.

The Cortex-M0+ processor equipped with this product integrates the MPU memory protection unit: provides hardware management and protection of memory, and controls access rights. In addition, it also integrates the MTB on-chip tracking unit: users can experience better tracking and debugging, optimized exception capture mechanism, and can locate bugs more quickly.

BAT32G179 uses an embedded ARM core, so it is compatible with all ARM tools and software.

5.2 Memory

5.2.1 Flash

BAT32G179 has a built-in flash memory that can be programmed, erased and rewritten. Has the following functions:

- Programs and data share 512K storage space.
- 20KB dedicated data Flash memory
- Support page erasing, each page size is 1024byte, erasing time 4ms
- Support byte/half-word/word (32bit) programming, programming time 24us

5.2.2 SRAM

BAT32G179 has built-in 64K bytes of embedded SRAM.

5.3 Enhanced DMA Controller

Built-in enhanced DMA (Direct Memory Access) controller can realize the function of data transfer between memories without using CPU.

- It supports the start of DMA through peripheral function interrupts, and can realize real-time control through communication, timer and A/D.
- The transmission source/destination area is optional for the entire address space range (when the flash area is used as the destination address, the flash needs to be preset to the programming mode).
- Supports 4 transfer modes (normal transfer mode, repetitive transfer mode, block transfer mode and chain transfer mode).

5.4 Linkage Controller

The linkage controller links each peripheral function output event with the peripheral function trigger source. So as to realize the coordinated operation between peripheral functions without using the CPU.

The linkage controller has the following functions:

The linkage controller has the following functions:

- The event signals can be linked together to realize the linkage of peripheral functions.
- 23 types of event input, 10 types of event trigger.

5.5 Clock Generation and Start

The clock generation circuit is a circuit that generates a clock for the CPU and peripheral hardware. There are the following 3 types of system clocks and clock oscillation circuits.

5.5.1 Main System Clock

- X1 oscillator circuit: It can generate 1-20MHz clock oscillation by connecting a resonator to the pins (X1 and X2), and can stop the oscillation by executing a deep sleep command or setting MSTOP.
- High-speed internal oscillator (high-speed OCO): The frequency can be selected for oscillation by the option byte. After the reset is released, the CPU defaults to start running with this high-speed internal oscillator clock. Oscillation can be stopped by executing a deep sleep instruction or setting the HIOSTOP bit. The frequency set by the option byte can be changed through the frequency selection register of the high-speed internal oscillator. The highest frequency is 64Mhz, and the accuracy is ±1.0%.
- Input the external clock from the pin (X2): (1~20MHz), and the input of the external main system clock can be disabled by executing the deep sleep instruction or setting the MSTOP bit.

5.5.2 Subsystem Clock

- XT1 oscillator circuit: It can generate 32.768KHz clock oscillation by connecting a 32.768KHz resonator to the pins (XT1 and XT2), and the oscillation can be stopped by setting the XTSTOP bit.
- Input the external clock from the pin (XT2): 32.768KHz, and the input of the external clock can be disabled by setting the XTSTOP bit.

5.5.3 Low-speed Internal Oscillator Clock

- Low-speed internal oscillator (low-speed OCO): generates 15KHz (TYP.) clock oscillation. The low-speed internal oscillator clock can be used as the CPU clock. The following peripheral hardware can be run by the low-speed internal oscillator clock:
- Watchdog timer (WWDT)
- Real Time Clock (RTC)
- 15-bit interval timer
- TimerA

5.5.4 PLL

- PLL: can be used as system clock. The source clock of the PLL can be either an external clock or an internal high-speed oscillator clock.

5.6 Power Management

5.6.1 Power Supply Mode

V_{DD}: external power supply, voltage range 1.8 to 5.5V
EV_{DD}: external power supply, voltage range 1.8 to 5.5V
The voltage of the V_{DD} pin must be equal to the voltage of the EV_{DD} pin.

5.6.2 Power-on Reset

The power-on reset circuit (POR) has the following functions:

- An internal reset signal is generated when the power is turned on. If the power supply voltage (V_{DD}) is greater than the detection voltage (V_{POR}), the reset is released. However, before reaching the operating voltage range, the reset state must be maintained through a voltage detection circuit or an external reset.
- The power supply voltage (V_{DD}) and the detection voltage (V_{PDR}) are compared. When $V_{DD}<V_{PDR}$, an internal reset signal is generated. However, when the power supply drops, it must be shifted to the deep sleep mode before it falls below the operating voltage range, or set to the reset state through a voltage detection circuit or an external reset. If you want to restart operation, you must confirm that the power supply voltage has returned to the operating voltage range.

5.6.3 Voltage Detection

The voltage detection circuit sets the operation mode and detection voltage (V_{LVDH}, V_{LVDL}, V_{LVD}) through the option byte. The voltage detection (LVD) circuit has the following functions:

- Compare the power supply voltage (V_{DD}) with the detection voltage (V_{LVDH}, V_{LVDL}, V_{LVD}) and generate an internal reset or interrupt request signal.
- The detection voltage of the power supply voltage (V_{LVDH}, V_{LVDL}, V_{LVD}) can select the detection level by the option byte.
- Can run in deep sleep mode.
- When the power supply rises, before reaching the operating voltage range, the reset state must be maintained through a voltage detection circuit or an external reset. When the power supply drops, it must be transferred to the deep sleep mode before being lower than the operating voltage range, or set to the reset state through a voltage detection circuit or an external reset.
- The operating voltage range varies according to the setting of the user option byte.

5.7 Low Power Consumption Mode

BAT32G179 supports two low-power modes to achieve the best compromise between low power consumption, short startup time, and available wake-up sources:

- Sleep mode: Enter the sleep mode by executing the sleep command. The sleep mode is a mode in which the CPU operating clock is stopped. Before setting the sleep mode, if the high-speed system clock oscillator circuit, high-speed internal oscillator, or subsystem clock oscillator circuit is oscillating, each clock continues to oscillate. Although this mode cannot reduce the operating current to the level of the deep sleep mode, it is an effective mode when you want to restart processing immediately through an interrupt request or when you want to perform intermittent operation frequently.
- Deep sleep mode: Enter the deep sleep mode by executing the deep sleep command. The deep sleep mode is a mode to stop the oscillation of the high-speed system clock oscillation circuit and the high-speed internal oscillator and stop the entire system. Can greatly reduce the operating current of the chip. Because the deep sleep mode can be cancelled by an interrupt request, intermittent operation is also possible. However, in the case of the X1 clock, because it is necessary to ensure the wait time for stable oscillation when releasing the deep sleep mode, if you must start processing immediately with an interrupt request, you must select the sleep mode.

In either mode, the registers, flags, and data memory all retain the contents before the standby mode, and also maintain the status of the output latch and output buffer of the input/output port.

5.8 Reset Function

The following 7 methods to generate a reset signal:

1) Input external reset through RESETB pin.
2) Generate an internal reset through the program runaway detection of the watchdog timer.
3) The internal reset is generated by comparing the power supply voltage of the power-on reset (POR) circuit and the detection voltage.
4) The internal reset is generated by comparing the power supply voltage of the voltage detection circuit (LVD) and the detection voltage.
5) Internal reset due to RAM parity error.
6) Internal reset due to access to illegal memory.
7) Software reset

The internal reset is the same as the external reset. After the reset signal is generated, the program is executed from the addresses written in addresses 0000H and 0001H.

5.9 Interrupt Function

The Cortex-M0+ processor has a built-in nested vectored interrupt controller (NVIC), which supports up to 32 interrupt request (IRQ) inputs and 1 non-maskable interrupt (NMI) input. In addition, the processor also supports multiple internal exceptions.

This product has expanded 32 maskable interrupt requests (IRQ) and 1 non-maskable interrupt (NMI), and can support up to 64 maskable interrupt sources and one non-maskable interrupt source. The actual number of interrupt sources varies from product to product.

		64-pin	80-pin	100-pin
Maskable Interrupt	external	13	13	13
	internal	33	44	58

5.10 Real Time Clock (RTC)

The real-time clock (RTC) has the following functions.

- Counter with year, month, week, day, hour, minute and second.
- Fixed period interrupt function (period: 0.5 second, 1 second, 1 minute, 1 hour, 1 day, 1 month)
- Alarm interrupt function (alarm clock: week, hour, minute)
- 1Hz pin output function
- Support the division of the subsystem clock or the main system clock as the running clock of the RTC
- The real-time clock interrupt signal (INTRTC) can be used as a wake-up from deep sleep mode
- Support a wide range of clock correction functions

Only when the sub-system clock (32.768KHz) or the divided frequency of the main system clock is selected as the running clock of the RTC, the year, month, week, day, hour, minute and second can be counted. When the low-speed internal oscillator clock (15KHz) is selected, only the fixed cycle interrupt function can be used.

5.11 Watchdog Timer

1 channel WWDT, 17bit watchdog timer is set to count operation by option byte. The watchdog timer runs on the low-speed internal oscillator clock (15KHz). The watchdog timer is used to detect program runaway. When a program out of control is detected, an internal reset signal is generated.

The following conditions are judged to be out of control of the program:

- When the watchdog timer counter overflows
- When a 1-bit operation instruction is executed on the enable register (WDTE) of the watchdog timer
- When writing data other than "ACH" to the WDTE register
- When writing data to the WDTE register while the window is closed

5.12 SysTick Timer

This timer is dedicated to the real-time operating system, but it can also be used as a standard down counter.

Its characteristics are: when the 24-bit down counter self-filling capacity counter reaches 0, a maskable system interrupt is generated.

5.13 Timer Timer4

This product has built-in timer unit timer4 which contains 4 16-bit timers. Each 16-bit timer is called a "channel", which can be used as an independent timer or combined with multiple channels for advanced timer functions.

5.13.1 Independent Channel Operation Function

The independent channel operation function is a function that can independently use any channel without being affected by the operation mode of other channels. The independent channel operation function can be used in the following modes:

1) Interval timer：Can be used as a reference timer that generates interrupts (INTTM) at regular intervals.
2) Square wave output：Whenever an INTTM interrupt is generated, a flip is triggered, and a square wave with a 50% duty cycle is output from the timer output pin (TO).
3) External event counter：Count the valid edge of the input signal of the timer input pin (TI), and if it reaches the specified number of times, it can be used as an event counter to generate an interrupt.
4) Frequency divider function (only limited to channel 0 of unit 0): divide the input clock of the timer input pin (TI00), and then output from the output pin (TO00).
5) Input pulse interval measurement: start counting at the valid edge of the input pulse signal of the timer input pin (TI) and capture the count value at the valid edge of the next pulse to measure the interval of the input pulse.
6) Measurement of the high/low level width of the input signal: start counting on one edge of the input signal of the timer input pin (TI) and capture the count value on the other edge to measure the high or low level of the input signal Width.
7) Delay counter: start counting at the valid edge of the input signal of the timer input pin (TI) and generate an interrupt after any delay period has elapsed.

5.13.2 Multi-channel Linkage Operation Function

Multi-channel linkage operation function can be realized by combining the master channel (the basic timer of the main control cycle) and the slave channel (the timer that follows the master control channel). Multi-channel linkage operation function can be used in the following modes:

1) One-shot pulse output: Use two channels in pairs to generate one-shot pulses that can set the output timing and pulse width arbitrarily.
2) PWM (Pulse Width Modulation) output: Use 2 channels in pairs to generate pulses with a period and duty cycle that can be set arbitrarily.
3) Multiple PWM (Pulse Width Modulation) output: It can generate up to 7 kinds of PWM signals with any duty cycle in a fixed cycle by expanding the PWM function and using 1 master channel and multiple slave channels.

5.13.3 8-bit Timer Operation Function

The 8-bit timer operation function can use the 16-bit timer channel as a function of two 8-bit timer channels. (Only channel 1 and channel 3 can be used)

5.13.4 LIN-bus Support Function

The timer4 unit can be used to check whether the received signal in LIN-bus communication is suitable for the LIN-bus communication format.

1) Wake-up signal detection: Start counting on the falling edge of the input signal of the UART serial data input pin (RxD) and capture the count value on the rising edge to measure the low-level width. If the low-level width is greater than or equal to a certain fixed value, it is considered as a wake-up signal.
2) Interval field detection: After detecting the wake-up signal, start counting from the falling edge of the input signal of the UART serial data input pin (RxD) and capture the count value on the rising edge to measure the low-level width. If the width of the low level is greater than or equal to a certain fixed value, it is regarded as an interval field.
3) Synchronous field pulse width measurement: After detecting the interval field, measure the low-level width and high-level width of the input signal of the UART serial data input pin (RxD). Calculate the baud rate based on the bit interval of the sync field measured in this way.

5.14 Timer Timer8

The 80-pin product adds a built-in timer unit timer8 with 8 16-bit timers. Each 16-bit timer is called a "channel", which can be used as an independent timer or combined with multiple channels for advanced timer functions.

5.14.1 Independent Channel Operation Function

The independent channel operation function is a function that can independently use any channel without being affected by the operation mode of other channels. The independent channel operation function can be used in the following modes:

1) Interval timer：Can be used as a reference timer that generates interrupts (INTTM) at regular intervals.
2) Square wave output：Whenever an INTTM interrupt is generated, a flip is triggered, and a square wave with a 50% duty cycle is output from the timer output pin (TO).
3) External event counter：Count the valid edge of the input signal of the timer input pin (TI), and if it reaches the specified number of times, it can be used as an event counter to generate an interrupt.
4) Input pulse interval measurement: start counting at the valid edge of the input pulse signal of the timer input pin (TI) and capture the count value at the valid edge of the next pulse to measure the interval of the input pulse.
5) Measurement of the high/low level width of the input signal: start counting on one edge of the input signal of the timer input pin (TI) and capture the count value on the other edge to measure the high or low level of the input signal Width.
6) Delay counter: start counting at the valid edge of the input signal of the timer input pin (TI) and generate an interrupt after any delay period has elapsed.

5.14.2 Multi-channel Linkage Operation Function

Multi-channel linkage operation function can be realized by combining the master channel (the basic timer of the main control cycle) and the slave channel (the timer that follows the master control channel). Multi-channel linkage operation function can be used in the following modes:

1) One-shot pulse output: Use two channels in pairs to generate one-shot pulses that can set the output timing and pulse width arbitrarily.
2) PWM (Pulse Width Modulation) output: Use 2 channels in pairs to generate pulses with a period and duty cycle that can be set arbitrarily.
3) Multiple PWM (Pulse Width Modulation) output: It can generate up to 7 kinds of PWM signals with any duty cycle in a fixed cycle by expanding the PWM function and using 1 master channel and multiple slave channels.

5.14.3 8-bit Timer Operation Function

The 8-bit timer operation function makes it possible to use a 16-bit timer channel in a configuration consisting of two 8-bit timer channels. This function can only be used for channels 1 and 3.

5.15 TimerA

This product has a built-in 16bit timer timerA, which is composed of a reload register and a down counter. It can be used in the following working modes:

- Timer mode: count the counting source (the counting source can be a clock or an external event)
- Pulse output mode: count the counting source and output pulse when overflow
- Event counter mode: An external event is counted. Operation is possible in DEEPSLEEP mode.
- Pulse width measurement mode: An external pulse width is measured.
- Pulse period measurement mode: An external pulse period is measured.

5.16 TimerM

The product contains 2 channels of 16-bit timer timerM optimized for motor control. It has the following 4 working modes:

- Timer mode:
  - Input capture function (Transfer the counter value to a register with an external signal as the trigger)
  - Output compare function (Detect register value matches with a counter, and Pin output can be changed at detection)
  - PWM function (Output pulse of any width continuously)
- Reset synchronous PWM mode: Output three-phase waveforms (6) without sawtooth wave modulation and dead time
- Complementary PWM mode: Output three-phase waveforms (6) with triangular wave modulation and dead time
- PWM3 mode: Output PWM waveforms (2) with a fixed period

5.17 TimerB

TimerB is a 16-bit timer, supports the following three modes:

- Timer mode:
  - Input capture function: Count at the rising edge, falling edge, or both rising/falling edges
  - Output compare function: Low output/high output/toggle output
- PWM mode: PWM output available with any duty cycle
- Phase counting mode: Automatic measurement available for the counts of the two-phase encoder

5.18 TimerC

This product has a built-in 16bit timer timerC, which can be triggered by software, comparator or timer timerM to realize the input capture function.

5.19 15-bit Interval Timer

This product has a built-in 15-bit interval timer, which can generate interrupts (INTIT) at any time interval set in advance, and can be used to wake up from deep sleep mode.

5.20 Clock Output/Buzzer Output Control Circuit

The clock output controller is used to provide the clock to the peripheral IC, and the buzzer output controller is used to output the square wave of the buzzer frequency. Clock output or buzzer output is realized by dedicated pins.

5.21 Universal Serial Communication Unit

This product has 4 built-in universal serial communication units, and each unit has up to 4 serial communication channels. It can realize the communication functions of standard SPI, simple SPI, UART and simple I^2C. Take the 80pin product as an example, the function allocation of each channel is as follows.

5.21.1 3-wire Serial Interface (Simple SPI)

Synchronize data transmission and reception with the serial clock (SCK) output from the master control device.

This is a clock synchronous communication interface that uses 1 serial clock (SCK), 1 sending serial data (SO), and 1 receiving serial data (SI) to communicate with a total of 3 communication lines.

[data transmission and reception]

- 7-bit or 8-bit data length
- Phase control of sending and receiving data
- MSB/LSB priority choice

[clock control]

- Choice of master control or slave
- Phase control of input/output clock
- The transmission cycle generated by the prescaler and the internal counter of the channel
- Maximum transfer rate

Master communication: Max.F_{CLK}/2

Slave communication: Max.F_{MCK}/6

[Interrupt function]

- Transmission end interrupt, buffer empty interrupt

[Error detection flag]

- Overflow error

5.21.2 Simple SPI With Slave Chip Select Function

SPI serial communication interface supporting slave chip select input function. This is a clock synchronization that uses a slave chip select input (SSI), a serial clock (SCK), a sending serial data (SO), and a receiving serial data (SI) 4 communication lines for communication. Communication Interface.

[Data sending and receiving]

- 7-bit or 8-bit data length
- Phase control of sending and receiving data
- MSB/LSB priority choice
- Level setting of sending and receiving data

[clock control]

- Phase control of input/output clock
- The transmission cycle generated by the prescaler and the internal counter of the channel
- Maximum transfer rate

Slave communication: Max.F_{MCK}/6

[Interrupt function]

- Transmission end interrupt, buffer empty interrupt

[Error detection flag]

- Overflow error

5.21.3 UART

The function of asynchronous communication through two lines of serial data transmission (TxD) and serial data reception (RxD). Use these two communication lines to send and receive data asynchronously (using the internal baud rate) with other communication parties according to the data frame (consisting of start bit, data, parity bit and stop bit). Full-duplex UART communication can be realized by using two channels dedicated for transmission (even-numbered channels) and dedicated for reception (odd-numbered channels), and LIN-bus can be supported by combining timer4 units and external interrupts (INTP0).

[Data sending and receiving]

- 7-bit, 8-bit or 9-bit data length
- MSB/LSB priority choice
- Selection of level setting and reverse phase of sending and receiving data
- Additional parity check bit, parity check function
- Additional stop bit, stop bit detection

[Interrupt function]

- Transmission end interrupt, buffer empty interrupt
- Error interrupt caused by framing error, parity error or overflow error

[Error detection flag]

- Frame error, parity error, overflow error

[LIN-bus function]

- Wake-up signal detection
- BF detection
- Measurement of synchronization field, calculation of baud rate

5.21.4 Simple I²C

The function of clock synchronization communication with multiple devices through two lines of serial clock (SCL) and serial data (SDA). Because this simple I²C is designed for single communication with flash memory, A/D converters and other devices, it can only be used as a master device. The start condition and stop condition are the same as the operation control register, and must comply with the AC characteristics and be processed by software.

[Data sending and receiving]

- Main control sending, main control receiving (only limited to the main control function of single main control)
- ACK output function, ACK detection function
- 8-bit data length (when sending the address, use the upper 7 bits to specify the address, and use the lowest bit for R/W control)
- Generate start and stop conditions through software

[interrupt function]

- End of transmission interrupt

[Error detection flag]

- ACK error, overflow error

[Functions not supported by simple I²C]

- Slave sending, slave receiving
- Multi-master control function (arbitration failure detection function)
- Waiting for detection function

5.22 Standard Serial Interface SPI

The serial interface SPI has the following 2 modes:

- Operation stop mode: This is a mode used when serial transmission is not performed, which can reduce power consumption.
- I^2C bus mode (supports multiple masters): This mode uses 3 lines of serial clock (SCK) and serial data bus (MISO and MOSI) to transmit 8-bit data with multiple devices.

5.23 Standard Serial Interface IICA

The serial interface IICA has the following 3 modes:

- Operation stop mode: This is a mode used when serial transmission is not performed, which can reduce power consumption.
- I^2C bus mode (supports multiple masters): This mode uses 2 lines of serial clock (SCLA) and serial data bus (SDAA) to transmit 8-bit data with multiple devices. In line with the I^2C bus format, the master device can generate "start condition", "address", "indication of the transfer direction", "data" and "stop condition" for the slave device on the serial data bus. The slave device automatically detects the received status and data through hardware. This function can simplify the I2C bus control part of the application. Because the SCLA pin and SDAA pin of the serial interface IICA are used as open-drain output, the serial clock line and the serial data bus require a pull-up resistor.
- Wake-up mode: In the deep sleep mode, when the extension code or the local station address from the autonomous control device is received, the deep sleep mode can be released by generating an interrupt request signal (INTIICA). Set through the IICA control register.

5.24 Controller CAN

This product can support up to 3 general CAN bus interfaces.

5.25 LCD BUS Interface

The LCD bus interface has the following functions:

- Support two different bus standards: 8080 mode, 6800 mode
- Support 8-bit/16-bit read and write operations
- Controllable transmission speed (up to 10MHz)
- When internal data transmission is enabled or external bus access is completed, DMA transmission can be triggered
- Support DMA read and write

5.26 Analog-to-digital Converter (ADC)

This product has a built-in 12-bit resolution analog-to-digital converter SARADC, which can convert analog input to digital value and supports up to 21 channels of ADC analog input (ANI0~ANI20). The ADC contains the following functions:

- 12-bit resolution, conversion rate 1.42Msps.
- Trigger mode: support software trigger, hardware trigger and hardware trigger in standby state
- Channel selection: support two modes of single-channel selection and multi-channel scanning
- Conversion mode: support single conversion and continuous conversion
- Working voltage: Support the working voltage range of $1.8V \leqslant V_{DD} \leqslant 5.5V$
- It can detect the built-in reference voltage (1.45V) and temperature sensor.

ADC can set various A/D conversion modes through the following mode combinations.

Trigger mode	Software trigger	Start the conversion by software operation.
	Hardware trigger no wait mode	Start the conversion by detecting the hardware trigger.
	Hardware trigger wait mode	In the conversion standby state with the power off, the power is turned on by detecting the hardware trigger, and the conversion starts automatically after the A/D power stabilization wait time.
Channel selection mode	Select mode	Select 1 channel of analog input for A/D conversion.
	Scan mode	Perform A/D conversion on 4 channels of analog input in sequence. It is possible to select 4 consecutive channels from ANI0 to ANI15 as analog input.
Conversion mode	Single conversion mode	Perform 1 A/D conversion on the selected channel.
	Continuous conversion mode	Perform continuous A/D conversion on the selected channel until it is stopped by software.
Sampling time/conversion time	Number of sampling clocks/number of conversion clocks	The sampling time can be set by the register. The default value of the sampling clock is 13.5 clk, and the Min value of the conversion clock is 31.5 clk.

5.27 Analog to Digital Conversion (DAC)

This product has a built-in 2-channel 8-bit resolution analog-to-digital converter DAC, which can convert digital input to analog signal. Has the following characteristics:

- 8-bit resolution D/A converter
- Support the output of two independent analog channels
- R-2R ladder method
- Built-in real-time output function

5.28 Programmable Gain Amplifier (PGA)

This product has two built-in programmable gain amplifiers (PGA0 and PGA1), which have the following functions:

- GAIN: X4, X8, X10, X12, X14, X16, X32
- The external pin (PGAGND) can be selected as the ground of the negative feedback resistance of the PGA (can be used as a differential mode)
- The output of PGA0 can be selected as analog input for A/D converter or analog input for positive terminal of comparator0 (CMP0).
- PGA1 output can be selected as analog input for A/D converter

5.29 Comparator (CMP)

This product has built-in two channels with hysteresis comparatorCMP0 and CMP1, with the following functions:

- The external input and reference multi-channels of CMP1 are optional.
- Can select external reference voltage input and internal reference voltage for reference voltage.
- The elimination width of the noise elimination digital filter can be selected.
- Can detect the valid edge of the comparator output and generate an interrupt signal.
- It can detect the valid edge of the comparator output and output the event signal to the linkage controller.

5.30 Two-wire Serial Debug Port (SW-DP)

ARM's SW-DP interface allows to connect to the microcontroller through a serial wire debugging tool.

5.31 Security Function

5.31.1 Flash CRC Calculation Function (High-speed CRC, general-purpose CRC)

Detect the data error of flash memory through CRC operation.

According to different purposes and conditions of use, the following 2 CRCs can be used respectively.

- High-speed CRC: In the initialization program, it can stop the operation of the CPU and check the entire code flash area at high speed。
- General CRC: In CPU operation, it is not limited to the code flash area but can be used for multi-purpose checking.

5.31.2 RAM Parity Error Detection Function

When reading RAM data, detect parity errors.

5.31.3 SFR Protection Function

Prevent the important SFR (Special Function Register) from being rewritten due to CPU runaway.

5.31.4 Illegal Memory Access Detection Function

Detect illegal access to illegal memory area (area without memory or area with restricted access).

5.31.5 Frequency Detection Function

Can use timer4 unit to self-check CPU or peripheral hardware clock frequency.

5.31.6 A/D Test Function

Perform A/D conversion on the A/D converter's positive (+) reference voltage, negative (-) reference voltage, analog input channel (ANI), temperature sensor output voltage, and internal reference voltage Self-test.

5.31.7 Digital Output Signal Level Detection Function of Input/ Output Port

When the input/output port is in output mode, the output level of the pin can be read.

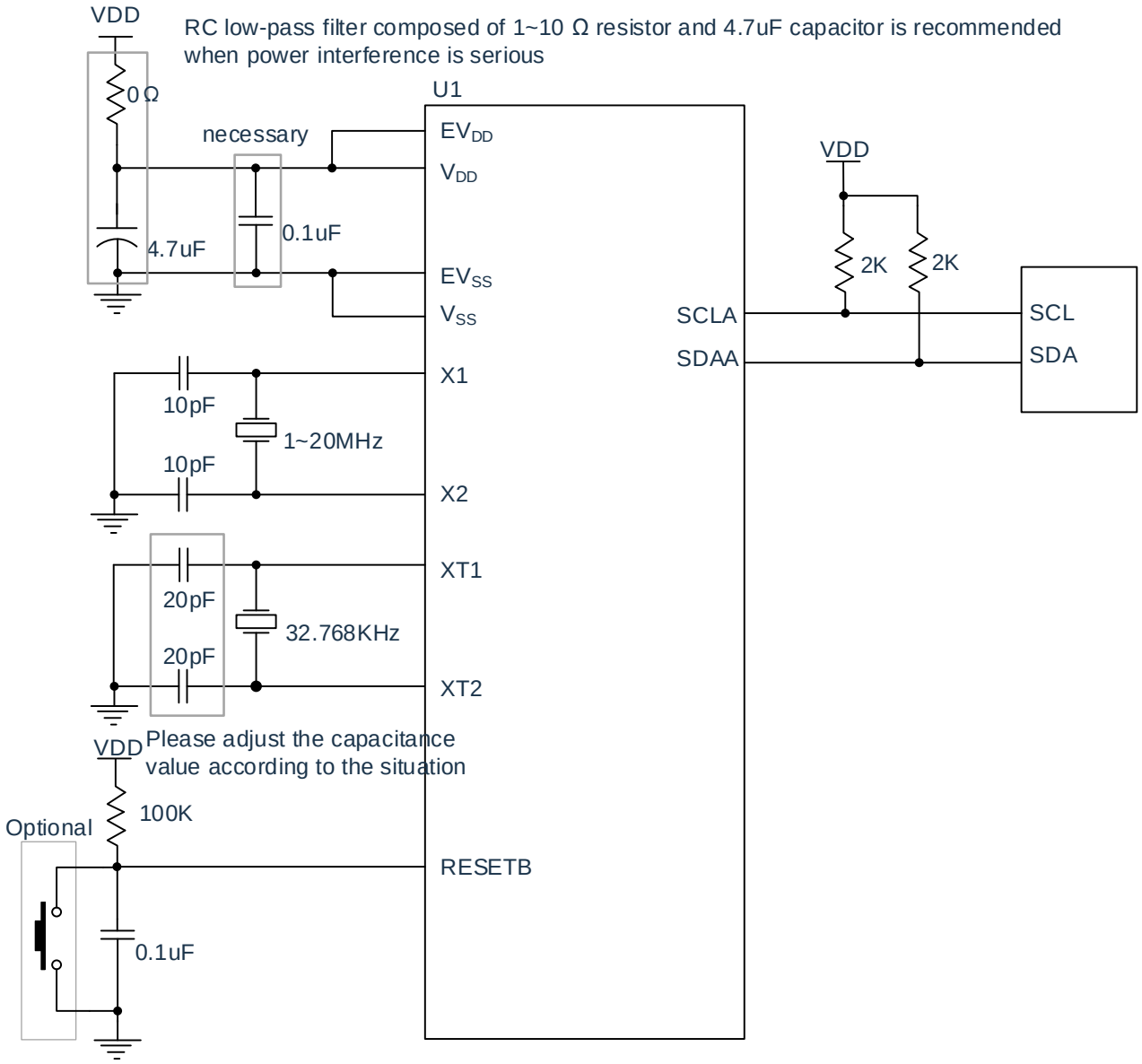
5.32 Key Function

The input pin (KR0~KR7) can be interrupted by the key to generate a key interrupt (INTKR).

6 Electrical Characteristics

6.1 Typical Application Peripheral Circuit

The device connection reference of the typical MCU application peripheral circuit is as follows:



6.2 Absolute Maximum Voltage Rating

(T_A= -40~105°C)

Item	Symbol	Condition	Rating	Unit
Source voltage	V_{DD}		-0.5~+6.5	V
	EV_{DD}		-0.5~+6.5	V
Input voltage	V_{I1}	P00~P06, P10~P17, P30, P31, P40~P47, P50~P57, P64~P67, P70~P77, P80~P87, P100~P102, P110~P111, P120, P130, P136, P140~P147	-0.3~EV_{DD}+0.3 and -0.3~V_{DD}+0.3 Note1	V
	V_{I2}	P60~P63(N-channel open drain)	-0.3~+6.5	V
	V_{I3}	P20~P27, P121~P124, P137, P150~P156, EXCLK, EXCLKS, RESETB	-0.3~V_{DD}+0.3 Note1	V
Output voltage	V_{O1}	P00~P06, P10~P17, P30, P31, P40~P47, P50~P57, P60~P67, P70~P77, P80~P87, P100~P102, P110~P111, P120, P130, P136, P140~P147	-0.3~EV_{DD}+0.3 and -0.3~V_{DD}+0.3 Note1	V
	V_{O2}	P20~P27, P137, P150~P156	-0.3~V_{DD}+0.3 Note1	V
Analog input voltage	V_{AI1}	ANI8~ANI20	-0.3~EV_{DD}+0.3 and -0.3~AV_{REF}(+)+0.3 Note1, 2	V
	V_{AI2}	ANI0~ANI7	-0.3~V_{DD}+0.3 and -0.3~AV_{REF}(+)+0.3 Note1, 2	V

Note1: Do not exceed 6.5V.

Note2: The pin of the A/D conversion target cannot exceed AV_{REF}(+)+0.3.

Note: Even if one of the items exceeds the absolute maximum rating for an instant, the quality of the product may be degraded. The absolute maximum rating is a rating that may cause physical damage to the product, and the product must be used under the condition that the rating is not exceeded.

Remark:

1. Unless otherwise specified, the characteristics of multiplexed pins are the same as those of port pins.
2. AV_{REF}(+): The positive (+) reference voltage of the A/D converter
3. Use V_{SS} as the reference voltage.

6.3 Absolute Maximum Current Rating

(T_A= -40~105°C)

Item	Symbol	Condition		Rating	Unit
High level output current	I_{OH1}	Each pin	P00~P06, P10~P17, P30, P31, P40~P47, P50~P57, P64~P67, P70~P77, P80~P87, P100~P102, P110~P111, P120, P130, P136, P137, P140~P147	-40	mA
		Total pins -170mA	P00~P04, P40~P45, P120, P130, P136, P137, P140~P144	-70	mA
			P05, P06, P10~P17, P30, P31, P50~P55, P64~P67, P70~P77, P100, P110~P111, P146, P147	-100	mA
	I_{OH2}	Each pin	P20~P27, P150~P156	-3	mA
		Total pins		-15	mA
Low-level output current	I_{OL1}	Each pin	P00~P06, P10~P17, P30, P31, P40~P47, P50~P57, P60~P67, P70~P77, P80~P87, P100~P102, P110~P111, P120, P130, P136, P137, P140~P147	40	mA
		Total pins 170mA	P00~P04, P40~P45, P120, P130, P136, P137, P140~P144	100	mA
			P05, P06, P10~P17, P30, P31, P50~P55, P60~P67, P70~P77, P100, P110~P111, P146, P147	120	mA
	I_{OL2}	Total pins	P20~P27, P150~P156	15	mA
		Total pins		45	mA
Working temperature	T_A	Normally run		-40~105	°C
		When flash programming			
Storage temperature	T_{stg}	-		-65~150	°C

Note: Even if one of the items exceeds the absolute maximum rating for an instant, the quality of the product may be degraded. The absolute maximum rating is a rating that may cause physical damage to the product, and the product must be used under the condition that the rating is not exceeded.

Remark: Unless otherwise specified, the characteristics of multiplexed pins are the same as those of port pins.

6.4 Oscillation Circuit Characteristics

6.4.1 X1, XT1 Characteristics

(T_A= -40~105℃, 1.8V≤V_{DD}≤5.5V, V_{SS}=0V)

Item	Resonator	Condition	Min	Typ	Max	Unit
X1 clock oscillation frequency (F_X)	Ceramic resonator/ crystal resonator	-	1.0	--	20.0	MHz
X1 clock oscillation stabilization time	Ceramic resonator/ crystal resonator	20MHz，C=10pF	-	15	-	ms
X1 clock oscillation feedback resistor	Ceramic resonator/ crystal resonator	-	0.6	-	1.8	MΩ
XT1 clock oscillation frequency (F_{XT})	Crystal resonator	-	32	32.768	35	KHz
XT1 clock oscillation stabilization time	Crystal resonator	32.768KHz，C=20pF	-	2	-	s

Note：

1. It only indicates the allowable frequency range of the oscillation circuit. Please refer to the AC characteristics for the command execution time.
2. Please entrust the resonator manufacturer to evaluate after installing the circuit, and use it after confirming the oscillation characteristics.

6.4.2 Internal Oscillator Characteristics

(T_A= -40~105℃， 1.8V≤V_{DD}≤5.5V, V_{SS}=0V)

Resonator	Condition	Min	Typ	Max	Unit
High-speed internal oscillator clock frequency (F_{IH})Note1,2	-	1.0	-	64.0	MHz
High speed internal oscillator stability time (T_{SU})	-	-	12	-	us
Clock frequency accuracy of high-speed internal oscillator	T_A =10~70℃	-1.0	-	+1.0	%
	T_A = 0~105℃	-1.5	-	+1.5	%
	T_A = -10~125℃	-2.0	-	+2.0	%
	T_A = -40~125℃	-4.0	-	+4.0	%
Clock frequency of low-speed internal oscillator (F_{IL})	-	12	15	18	KHz

Note：

1. Select the frequency of the high-speed internal oscillator by the option byte.
2. It only shows the characteristics of the oscillation circuit, please refer to the AC characteristics for the command execution time.

6.4.3 PLL Oscillator Characteristics

(T_A= -40~105℃, 1.8V≤V_{DD}≤5.5V, V_{SS}=0V)

Resonator	Condition	Min	Typ	Max	Unit
PLL input frequency Note1	-	4.0	-	8.0	MHz
PLL lock time	-	40	-	-	us

Note1：It only shows the characteristics of the oscillation circuit, please refer to the AC characteristics for the command execution time.

6.5 DC Characteristics

6.5.1 Pin Characteristics

(T_A= -40~105℃, 1.8V≤EV_{DD}=V_{DD}≤5.5V, V_{SS}=EV_{SS}=0V)

Item	Symbol	Condition		Min	Typ	Max	Unit
High leveloutput Current Note1	I_{OH1}	P00~P06, P10~P17, P30, P31, P40~P47, P50~P57, P64~P67, P70~P77, P80~P87, P100~P102, P110~P111, P120, P130, P136, P137, P140~P147 pin alone	1.8V≤EV_{DD}≤5.5V -40~85℃	-	-	-12.0 Note2	mA
			1.8V≤EV_{DD}≤5.5V 85~105℃	-	-	-6.0 Note2	
		P00~P04, P40~P45, P120, P130, P136, P137, P140~P144 Total pins (when duty cycle ≤70% Note3)	4.0V≤EV_{DD}≤5.5V -40~85℃	-	-	-60.0	mA
			4.0V≤EV_{DD}≤5.5V 85~105℃	-	-	-30.0	
			2.4V≤EV_{DD}<4.0V	-	-	-12.0	mA
			1.8V≤EV_{DD}<2.4V	-	-	-6.0	mA
		P05, P06, P10~P17, P30, P31, P50~P55, P64~P67, P70~P77, P100, P110~P111, P146, P147 Total pins (when duty cycle ≤70% Note3)	4.0V≤EV_{DD}≤5.5V -40~85℃	-	-	-80.0	mA
			4.0V≤EV_{DD}≤5.5V 85~105℃	-	-	-30.0	
			2.4V≤EV_{DD}<4.0V	-	-	-20.0	mA
			1.8V≤EV_{DD}<2.4V	-	-	-10.0	mA
		Total pins (when duty cycle ≤70% Note3)	1.8V≤EV_{DD}≤5.5V -40~85℃	-	-	-140.0	mA
			1.8V≤EV_{DD}≤5.5V 85~105℃	-	-	-60.0	
	I_{OH2}	P20 ~ P27, P150~P156 1 pin alone	1.8V≤V_{DD}≤5.5V	-	-	-2.5 Note2	mA
		Total pins (when duty cycle ≤70% Note3)	1.8V≤V_{DD}≤5.5V	-	-	-10	mA

Note1: This is the current value that guarantees the operation of the device even if current flows from the EV_{DD}, V_{DD} pin to the output pin.

Note2: Can not exceed the total current value.

Note3: This is the output current value of "duty cycle≤70%condition".

To change the output current value with a duty cycle ＞ 70% can be calculated with the following calculation formula (when the duty cycle is changed to n%).

The total output current of the pins = (I_{OH}×0.7)/(n×0.01)

＜example＞ I_{OH} = -10.0mA, n =80%

The total output current of the pins = (-10.0×0.7)/(80×0.01) ≈ -8.7mA

The current of each pin does not change due to the duty cycle, and no current above the absolute maximum rating will flow.

Note: In the N-channel open-drain mode, the pin set to the N-channel open-drain valid does not output a high level.

Remark: Unless otherwise specified, the characteristics of multiplexed pins are the same as those of port pins.

(T_A= -40~105℃, 1.8V≤EV_{DD}=V_{DD}≤5.5V, V_{SS}=EV_{SS}=0V)

Item	Symbol	Condition		Min	Typ	Max	Unit
Low-level output current[Note1]	I_{OL1}	P00~P06, P10~P17, P30, P31, P40~P47, P50~P57, P60~P67, P70~P77, P80~P87, P100~P102, P110~P111, P120, P130, P136, P137, P140~P147 pin alone	1.8V≤EV_{DD}≤5.5V -40~85℃	-	-	30[Note2]	mA
			1.8V≤EV_{DD}≤5.5V 85~105℃	-	-	15[Note2]	
		P00~P04, P40~P45, P120, P130, P136, P137, P140~P144 Total pins (when duty cycle ≤70%[Note3])	4.0V≤EV_{DD}≤5.5V -40~85℃	-	-	100	mA
			4.0V≤EV_{DD}≤5.5V 85~105℃	-	-	50	
			2.4V≤EV_{DD}<4.0V	-	-	30	mA
			1.8V≤EV_{DD}<2.4V	-	-	15	mA
		P05, P06, P10~P17, P30, P31, P50~P55, P60~P67, P70~P77, P100, P110~P111, P146, P147 Total pins (when duty cycle ≤70%[Note3])	4.0V≤EV_{DD}≤5.5V -40~85℃	-	-	120	mA
			4.0V≤EV_{DD}≤5.5V 85~105℃	-	-	60	
			2.4V≤EV_{DD}<4.0V	-	-	40	mA
			1.8V≤EV_{DD}<2.4V	-	-	20	mA
		Total pins (when duty cycle ≤70%[Note3])	1.8V≤EV_{DD}≤5.5V -40~85℃	-	-	150	mA
			1.8V≤EV_{DD}≤5.5V 85~105℃	-	-	80	
	I_{OL2}	P20~P27, P150~P156 1 pin alone	1.8V≤V_{DD}≤5.5V	-	-	6[Note2]	mA
		Total pins (when duty cycle ≤70%[Note3])	1.8V≤V_{DD}≤5.5V	-	-	40	mA

Note1: This is the current value that guarantees the operation of the device even if current flows from the output pin to the EV_{SS} and V_{SS} pins.

Note2: Can not exceed the total current value.

Note3: This is the output current value of "duty cycle≤70% condition"。

The output current value with a duty cycle ＞ 70% can be calculated with the following calculation formula (when the duty cycle is changed to n%)

• The total output current of the pins = (I_{OL}×0.7)/(n×0.01)

＜example＞ I_{OL}= 10.0mA, n = 80%

The total output current of the pins = (10.0×0.7)/(80×0.01) ≈ 8.7mA

The current of each pin does not change due to the duty cycle, and no current above the absolute maximum rating will flow.

Remark: Unless otherwise specified, the characteristics of multiplexed pins are the same as those of port pins.

(T_A= -40~105℃, 1.8V≤EV_{DD}=V_{DD}≤5.5V, V_{SS}=EV_{SS}=0V)

Item	Symbol	Condition		Min	Typ	Max	Unit
High level input voltage	V_{IH1}	P00~P06, P10~P17, P30, P31, P40~P47, P50~P57, P64~P67, P70~P77, P80~P87, P100~P102, P110~P111, P120, P136, P140~7P147	Schmidt input	0.8EV_{DD}	-	EV_{DD}	V
	V_{IH2}	P01, P03, P04, P10, P14~P17, P30, P43~P44, P50, P55, P142~P143	TTL input 4.0V≤EV_{DD}≤5.5V	2.2	-	EV_{DD}	V
			TTL input 3.3V≤EV_{DD}<4.0V	2.0	-	EV_{DD}	V
			TTL input 1.8V≤EV_{DD}<3.3V	1.5	-	EV_{DD}	V
	V_{IH3}	P20~P27, P137, P150~P156		0.7V_{DD}	-	V_{DD}	V
	V_{IH4}	P60~P63		0.7EV_{DD}	-	6.0	V
	V_{IH5}	P121~P124, EXCLK, EXCLKS, RESETB		0.8V_{DD}	-	V_{DD}	V
Low-level input voltage	V_{IL1}	P00~P06, P10~P17, P30, P31, P40~P47, P50~P57, P64~P67, P70~P77, P80~P87, P100~P102, P110~P111, P120, P136, P140~P147	Schmidt input	0	-	0.2EV_{DD}	V
	V_{IL2}	P01, P03, P04, P10, P14~P17, P30, P43~P44, P50, P55, P142~P143	TTL input 4.0V≤EV_{DD}≤5.5V	0	-	0.8	V
			TTL input 3.3V≤EV_{DD}<4.0V	0	-	0.5	V
			TTL input 1.8V≤EV_{DD}<3.3V	0	-	0.32	V
	V_{IL3}	P20~P27, P137, P150~P156		0	-	0.3V_{DD}	V
	V_{IL4}	P60~P63		0	-	0.3EV_{DD}	V
	V_{IL5}	P121~P124, EXCLK, EXCLKS, RESETB		0	-	0.2V_{DD}	V

Note: Even in the N-channel open-drain mode, the maximum V_{IH} (MAX.) of the pin that is set to the N-channel open-drain is also EV_{DD}.

Remark: Unless otherwise specified, the characteristics of multiplexed pins are the same as those of port pins.

(T_A= -40~105℃, 1.8V≤EV_{DD}=V_{DD}≤5.5V, V_{SS}=EV_{SS}=0V)

Item	Symbol	Condition		Min	Typ	Max	Unit
High level output voltage	V_{OH1}	P00~P06, P10~P17, P30, P31, P40~P47, P50~P57, P64~P67, P70~P77, P80~P87, P100~P102, P110~P111, P120, P130, P136, P137, P140~P147	4.0V≤EV_{DD}≤5.5V、I_{OH1}= -12.0mA	EV_{DD}-1.5	-	-	V
			4.0V≤EV_{DD}≤5.5V、I_{OH1}= -6.0mA	EV_{DD}-0.7	-	-	V
			2.4V≤EV_{DD}≤5.5V、I_{OH1}= -3.0mA	EV_{DD}-0.6	-	-	V
			1.8V≤EV_{DD}≤5.5V、I_{OH1}= -2mA	EV_{DD}-0.5	-	-	V
	V_{OH2}	P20~P27, P150~P156	4.0V≤V_{DD}≤5.5V、I_{OH2}= -2.5mA	EV_{DD}-1.5	-	-	V
			4.0V≤V_{DD}≤5.5V、I_{OH2}= -1.5mA	EV_{DD}-0.7	-	-	V
			2.4V≤V_{DD}≤5.5V、I_{OH2}= -0.5mA	EV_{DD}-0.6	-	-	V
			1.8V≤V_{DD}≤5.5V、I_{OH2}= -0.4mA	V_{DD}-0.5	-	-	V
Low-level output voltage	V_{OL1}	P00~P06, P10~P17, P30, P31, P40~P47, P50~P57, P60~P67, P70~P77, P80~P87, P100~P102, P110~P111, P120, P130, P136, P137, P140~P147	4.0V≤EV_{DD}≤5.5V、I_{OL1}=35.0mA	-	-	1.2	V
			4.0V≤EV_{DD}≤5.5V、I_{OL1}=20.0mA	-	-	0.7	V
			2.4V≤EV_{DD}≤5.5V、I_{OL1}=9.0mA	-	-	0.4	V
			1.8V≤EV_{DD}≤5.5V、I_{OL1}=7.0mA	-	-	0.4	V
	V_{OL2}	P20~P27, P150~P156	4.0V≤V_{DD}≤5.5V、I_{OL2}=10.0mA	-	-	1.2	V
			4.0V≤V_{DD}≤5.5V、I_{OL2}=6.0mA	-	-	0.7	V
			2.4V≤V_{DD}≤5.5V、I_{OL2}=2.5mA	-	-	0.4	V
			1.8V≤V_{DD}≤5.5V、I_{OL2}=2.0mA	-	-	0.4	V

Note: In the N-channel open-drain mode, the pin set to the N-channel open-drain valid does not output a high level.

Remark: Unless otherwise specified, the characteristics of multiplexed pins are the same as those of port pins.

(T_A= -40~105℃, 1.8V≤EV_{DD}=V_{DD}≤5.5V, V_{SS}=EV_{SS}=0V)

Item	Symbol	Condition		Min	Typ	Max	Unit
High-level input leakage current	I_{LIH1}	P00~P06, P10~P17, P30, P31, P40~P47, P50~P57, P60~P67, P70~P77, P80~P87, P100~P102, P110~P111, P120, P130, P136, P140~P147	V_I=EV_{DD}	-	-	1	uA
	I_{LIH2}	P20~P27, P137, P150~P156, RESETB	V_I=V_{DD}	-	-	1	uA
	I_{LIH3}	P121~P124 (X1, X2, EXCLK, XT1, XT2, EXCLKS)	V_I=V_{DD}, when input port and external clock input	-	-	1	uA
			V_I=V_{DD}, when the resonator is connected	-	-	10	uA
Low-level input leakage current	I_{LIL1}	P00~P06, P10~P17, P30, P31, P40~P47, P50~P57, P60~P67, P70~P77, P80~P87, P100~P102, P110~P111, P120, P130, P136, P140~P147	V_I=EV_{SS}	-	-	-1	uA
	I_{LIL2}	P20~P27, P137, P150~P156, RESETB	V_I=V_{SS}	-	-	-1	uA
	I_{LIL3}	P121~P124 (X1, X2, EXCLK, XT1, XT2, EXCLKS)	V_I=V_{SS}, when input port and external clock input	-	-	-1	uA
			V_I=V_{SS}, when the resonator is connected	-	-	-10	uA
Internal pull-up resistor	R_U	P00~P06, P10~P17, P30, P31, P40~P45, P50~P57, P64~P67, P70~P77, P80~P87, P100~P102, P110~P111, P120, P136, P137, P140~P147	V_I=EV_{SS}, when input port	10	30	100	kΩ

Remark: Unless otherwise specified, the characteristics of multiplexed pins are the same as those of port pins.

6.5.2 Power Supply Current Characteristics

(T_A= -40~105℃, 1.8V≤EV_{DD}=V_{DD}≤5.5V, V_{SS}=EV_{SS}=0V)

Item	Symbol	Condition				Min	Typ	Max	Unit
current Note1	I_{DD1}	Operating mode	High-speed internal oscillator	F_{HOCO}=64MHz, F_{IH}=64MHz Note3		-	7.5	14	mA
				F_{HOCO}=48MHz, F_{IH}=48MHz Note3		-	7.5	12	
				F_{HOCO}=32MHz, F_{IH}=32MHz Note3		-	9	11	
			High-speed main system clock	F_{MX}=20MHz Note2	Input square wave	-	6	8	mA
					Connect the crystal	-	6	8	
			Subsystem clock operation	F_{SUB}=32.768 KHz Note4	Input square wave	-	85	150	uA
					Connect the crystal	-	85	150	
	I_{DD2}	Sleep mode	High-speed internal oscillator	F_{HOCO}=64MHz, F_{IH}=64MHz Note3		-	2.4	8	mA
				F_{HOCO}=48MHz, F_{IH}=48MHz Note3		-	1.8	6	
				F_{HOCO}=32MHz, F_{IH}=32MHz Note3		-	1.2	4	
			High-speed main system clock	F_{MX}=20MHz Note2	Input square wave	-	1	3	mA
					Connect the crystal	-	1	3	
			Subsystem clock operation	F_{SUB}=32.768 KHz Note5	Input square wave	-	1.8	40	uA
					Connect the crystal	-	1.8	40	
	I_{DD3} Note 6	Deep sleep mode Note7	T_A= -40℃~25℃ V_{DD}=3.0V			-	1.5	2.4	uA
			T_A= -40℃~85℃ V_{DD}=3.0V			-	1.5	25	
			T_A= -40℃~105℃ V_{DD}=3.0V			-	1.5	35	

Note1: Total current flowing into V_{DD} and EV_{DD}, including the input leakage current flowing when the level of the input pin is fixed to V_{DD}, EV_{DD} or V_{SS}, EV_{SS}. The values of the TYP. column include the current of the CPU executing the multiplication instruction (I_{DD1}),not including the peripheral operation current. The values below the MAX. column include the current of the CPU executing the multiplication instruction (I_{DD1}) and the peripheral operation current.However, not including the current flowing into the A/D converter, LVD circuit, I/O port, and on-chip pull-up/pull-down resistors and the current flowing during data flash rewrite.

Note2: This is the case when the high-speed internal oscillator and the subsystem clock stop oscillating.

Note3: This is the case where the high-speed main system clock and subsystem clock stop oscillating.

Note4: This is the case when the high-speed internal oscillator and the high-speed main system clock stop oscillating.

Note5: This is the case when the high-speed internal oscillator and the high-speed main system clock stop oscillating. Contains the current flowing to the RTC, but does not include the 15-bit interval timer and watchdog timer current

Note6: Does not include current to RTC, 15-bit interval timer and watchdog timer.

Note7: For the current value when the subsystem clock is running in the deep sleep mode, please refer to the current value when the subsystem clock is running in the sleep mode.

Note:

1. F_{HOCO}: The clock frequency of the high-speed internal oscillator, F_{IH}: the system clock frequency provided by the high-speed internal oscillator.
2. F_{SUB} ： External subsystem clock frequency (XT1/XT2 clock oscillation frequency).
3. F_{MX}: External main system clock frequency (X1/X2 clock oscillation frequency).
4. TYP. The temperature condition of the value is T_A=25°C.

(T_A= -40~105℃, 1.8V≤EV_{DD}=V_{DD}≤5.5V, V_{SS}=EV_{SS}=0V)

Parameter	Symbol	Condition		Min	Typ	Max	Unit
Low-speed internal oscillator operating current	I_{FIL} Note1	-		-	0.2	-	uA
RTC operating current	I_{RTC} Note1,2,3	-		-	0.04	-	uA
15-bit interval timer operating current	I_{IT} Note 1,2,4	-		-	0.02	-	uA
Watchdog timer operating current	I_{WDT} Note 1,2,5	F_{IL}=15KHz		-	0.22	-	uA
A/D converter operating current	I_{ADC} Note 1,6	ADC HS mode @64MHz		-	2.2	-	mA
		ADC HS mode @4MHz		-	1.3	-	mA
		ADC LC mode @24MHz		-	1.1	-	mA
		ADC LC mode @4MHz		-	0.8	-	mA
D/A converter operating current	I_{DAC} Note 1,8	Each channel		-	1.4	-	mA
PGA operating current		Each channel		-	480	700	uA
comparator operating current	I_{CMP} Note 1,9	Each channel	Does not use internal reference voltage	-	60	100	uA
			Use internal reference voltage	-	80	140	uA
LVD operating current	I_{LVD} Note 1,7	-		-	0.08	-	uA

Note1: This is the current flowing through V_{DD}.

Note2: This is the case when the high-speed internal oscillator and the high-speed system clock stop oscillating。

Note3: This is the current that only flows to the real-time clock (RTC) (not including the operating current of the low-speed internal oscillator and XT1 oscillator circuit). When the real-time clock is running in running mode or sleep mode, the current value of the microcontroller is I_{DD1} or I_{DD2} plus the value of I_{RTC}. In addition, when low-speed internal oscillator is selected, I_{FIL} must be added. I_{DD2} when the subsystem clock is running contains the operating current of the real-time clock.

Note4: This is the current that only flows to the 15-bit interval timer (not including the operating current of the low-speed internal oscillator and XT1 oscillator circuit). When the 15-bit interval timer is running in run mode or sleep mode, the current value of the microcontroller is the value of I_{DD1} or I_{DD2} plus I_{IT}. In addition, when low-speed internal oscillator is selected, I_{FIL} must be added.

Note5: This is the current that only flows to the watchdog timer (including the operating current of the low-speed internal oscillator). When the watchdog timer is running, the current value of the microcontroller is I_{DD1} or I_{DD2} or I_{DD3} plus the value of I_{WDT}.

Note6: This is the current that only flows to the A/D converter. When the A/D converter is running in running mode or sleep mode, the current value of the microcontroller is I_{DD1} or I_{DD2} plus the value of I_{ADC}.

Note7: This is the current that only flows to the LVD circuit. In the case of LVD circuit operation, the current value of the microcontroller is the value of I_{DD1} or I_{DD2} or I_{DD3} plus I_{LVD}.

Note8: This is the current that only flows to the D/A converter. When the A/D converter is running in running mode or sleep mode, the current value of the microcontroller is I_{DD1} or I_{DD2} plus the value of I_{ADC}.

Note9: This is the current that only flows to the comparator circuit. When the comparator circuit is running, the current value of the microcontroller is the value of I_{DD1} or I_{DD2} or I_{DD3} plus I_{CMP}.

Note:

1. F_{IL}: Clock frequency of low-speed internal oscillator.
2. TYP. The temperature condition of the value is T_A=25℃.

6.6 AC Characteristic

(T_A= -40~105℃, 1.8V≤EV_{DD}=V_{DD}≤5.5V, V_{SS}=EV_{SS}=0V)

Item	Symbol	Condition		Min	Typ	Max	Unit
Instruction cycle (Minimum instruction execution time)	T_{CY}	The main system clock (F_{MAIN}) runs	1.8V≤V_{DD}≤5.5V	0.015625	-	1	us
		Subsystem clock (F_{SUB}) operation	1.8V≤V_{DD}≤5.5V	28.5	30.5	31.3	us
External system clock frequency	F_{EX}	1.8V≤V_{DD}≤5.5V		1.0	-	20.0	MHz
	F_{EXS}	1.8V≤V_{DD}≤5.5V		32.0	-	35.0	KHz
High and low level width of external system clock input	T_{EXH} T_{EXL}	1.8V≤V_{DD}≤5.5V		24	-	-	ns
	T_{EXHS} T_{EXLS}	1.8V≤V_{DD}≤5.5V		13.7	-	-	us
TI00 ~ TI03, TI10 ~ TI17 output frequency	T_{TIH} T_{TIL}	1.8V≤V_{DD}≤5.5V		1/F_{MCK}+10	-	-	ns
Input period of timer timerA	T_C	T_{AIO}	2.4V≤EV_{DD}≤5.5V	100	-	-	ns
			1.8V≤EV_{DD}<2.4V	300	-	-	ns
The high and low level width of timerA input	T_{TAIH} T_{TAIL}	T_{AIO}	2.4V≤EV_{DD}≤5.5V	40	-	-	ns
			1.8V≤EV_{DD}<2.4V	120	-	-	ns

Note: F_{MCK}: timer4, timer8 operating clock frequency of timer4 unit

(T_A= -40~105℃, 1.8V≤EV_{DD}=V_{DD}≤5.5V, V_{SS}=EV_{SS}=0V)

Item	Symbol	Condition		Min	Typ	Max	Unit
Timer M input high and low level width	T_{TMIH} T_{TMIL}	TMIOA0, TMIOA1, TMIOB0, TMIOB1, TMIOC0, TMIOC1, TMIOD0, TMIOD1		3/F_{CLK}	-	-	ns
Timer M forced cut-off signal input low-level width	T_{TMSIL}	P136/INTP0	2MHz＜F_{CLK}≤48MHz	1	-	-	us
			F_{CLK}≤2MHz	1/F_{CLK}+1	-	-	us
Timer B input high and low level width	T_{TBIH} T_{TBIL}	TBIOA, TBIOB		2.5/F_{CLK}	-	-	ns
TO00 ~ TO03, TO10 ~ TO17, TAIO0, TAO0, TMIOA0, TMIOA1, TMIOB0, TMIOB1, TMIOC0, TMIOC1, TMIOD0, TMIOD1, TBIOA, TBIOB Output frequency	F_{TO}	4.0V≤EV_{DD}≤5.5V		-	-	16	MHz
		2.4V≤EV_{DD}＜4.0V		-	-	8	MHz
		1.8V≤EV_{DD}＜2.4V		-	-	4	MHz
CLKBUZ0, CLKBUZ1 Output frequency	F_{PCL}	4.0V≤EV_{DD}≤5.5V		-	-	16	MHz
		2.4V≤EV_{DD}＜4.0V		-	-	8	MHz
		1.8V≤EV_{DD}＜2.4V		-	-	4	MHz
High and low level width of interrupt input	T_{INTH} T_{INTL}	INTP0 ~ INTP11	1.8V≤EV_{DD}≤5.5V	1	-	-	us
High and low level width of key interrupt input	T_{KR}	KR0 ~ KR7	1.8V≤EV_{DD}≤5.5V	250	-	-	ns
RESETB low-level width	T_{RSL}	-		10	-	-	us

6.7 Peripheral Features

6.7.1 Universal Interface Unit

1) UART mode

(T_A= -40~105℃, 1.8V≤EV_{DD}=V_{DD}≤5.5V, V_{SS}=EV_{SS}=0V)

Item	Condition		Specification Value		Unit
			Min	Max	
Transfer rate	1.8V≤EV_{DD}≤5.5V		-	F_{MCK}/6	bps
		The theoretical value of the maximum transfer rate F_{MCK}=F_{CLK}	-	10.6	Mbps

(T_A= 85~105℃, 1.8V≤EV_{DD}=V_{DD}≤5.5V, V_{SS}=EV_{SS}=0V)

Item	Condition		Specification Value		Unit
			Min	Max	
Transfer rate	1.8V≤EV_{DD}≤5.5V		-	F_{MCK}/12	bps
		Theoretical value of the maximum transfer rate F_{MCK}=F_{CLK}	-	5.3	Mbps

2) Three-wire SPI mode (master mode, internal clock output)

(T_A= -40~105℃, 1.8V≤EV_{DD}=V_{DD}≤5.5V, V_{SS}=EV_{SS}=0V)

Item	Symbol	Condition		-40 ~ 85℃		85 ~ 105℃		Unit
				Min	Max	Min	Max	
SCLKp cycle time	T_{KCY1}	T_{KCY1}≥2/F_{CLK}	4.0V≤EV_{DD}≤5.5V	31.25	-	62.5	-	ns
			2.7V≤EV_{DD}≤5.5V	41.67	-	83.33	-	ns
			2.4V≤EV_{DD}≤5.5V	65	-	125	-	ns
			1.8V≤EV_{DD}≤5.5V	125	-	250	-	ns
SCLKp high/low level width	T_{KH1} T_{KL1}	4.0V≤EV_{DD}≤5.5V		T_{KCY1}/2-4	-	T_{KCY1}/2-7	-	ns
		2.7V≤EV_{DD}≤5.5V		T_{KCY1}/2-5	-	T_{KCY1}/2-10	-	ns
		2.4V≤EV_{DD}≤5.5V		T_{KCY1}/2-10	-	T_{KCY1}/2-20	-	ns
		1.8V≤EV_{DD}≤5.5V		T_{KCY1}/2-19	-	T_{KCY1}/2-38	-	ns
SDIp preparation time (to SCLKp↑)	T_{SIK1}	4.0V≤EV_{DD}≤5.5V		12	-	23	-	ns
		2.7V≤EV_{DD}≤5.5V		17	-	33	-	ns
		2.4V≤EV_{DD}≤5.5V		20	-	38	-	ns
		1.8V≤EV_{DD}≤5.5V		28	-	55	-	ns
SDIp hold time (to SCLKp↑)	T_{KSI1}	1.8V≤EV_{DD}≤5.5V		5	-	10	-	ns
SCLKp↓→ SDOp output delay time	T_{KSO1}	1.8V≤EV_{DD}≤5.5V C=20pF Note1		-	5	-	10	ns

Note1: C is the load capacitance of the SCLKp and SDOp output lines。

Note: Through the port inputmode register and the port outputmode register, the SDIp pin is selected as the normal input buffer and theSDOp the pin and SCLKp pin are selected as the usual output mode.

Remark: It is guaranteed by the design and not tested in mass production.

3) Three-wire SPImode (slave mode, external clock input)

(T_A= -40~105℃, 1.8V≤EV_{DD}=V_{DD}≤5.5V, V_{SS}=EV_{SS}=0V)

Item	Symbol	Condition		-40 ~ 85℃		85 ~ 105℃		Unit
				Min	Max	Min	Max	
SCLKp cycle time	T_{KCY2}	4.0V≤EV_{DD}≤5.5V	20MHz＜F_{MCK}	8/F_{MCK}	-	16/F_{MCK}	-	ns
			F_{MCK}≤20MHz	6/F_{MCK}	-	12/F_{MCK}	-	ns
		2.7V≤EV_{DD}≤5.5V	16MHz＜F_{MCK}	8/F_{MCK}	-	16/F_{MCK}	-	ns
			F_{MCK}≤16MHz	6/F_{MCK}	-	12/F_{MCK}	-	ns
		2.4V≤EV_{DD}≤5.5V		6/F_{MCK} and≥500	-	12/F_{MCK} and≥1000	-	ns
		1.8V≤EV_{DD}≤5.5V		6/F_{MCK} and≥750	-	12/F_{MCK} and≥1500	-	ns
SCLKp high/low level width	T_{KH2} T_{KL2}	4.0V≤EV_{DD}≤5.5V		T_{KCY1}/2-7	-	T_{KCY1}/2-14	-	ns
		2.7V≤EV_{DD}≤5.5V		T_{KCY1}/2-8	-	T_{KCY1}/2-16	-	ns
		1.8V≤EV_{DD}≤5.5V		T_{KCY1}/2-18	-	T_{KCY1}/2-36	-	ns
SDIp preparation time (to SCLKp↑)	T_{SIK2}	2.7V≤EV_{DD}≤5.5V		1/F_{MCK}+20	-	1/F_{MCK}+40	-	ns
		1.8V≤EV_{DD}≤5.5V		1/F_{MCK}+30	-	1/F_{MCK}+60	-	ns
SDIp hold time (to SCLKp↑)	T_{KSI2}	1.8V≤EV_{DD}≤5.5V		1/F_{MCK}+31	-	1/F_{MCK}+62	-	ns
SCLKp↓→ SDOp output delay time	T_{KSO2}	2.7V≤EV_{DD}≤5.5V C=30pF Note1		-	2/F_{MCK}+ 44	-	2/F_{MCK} +66	ns
		2.4V≤EV_{DD}≤5.5V C=30pF Note1		-	2/F_{MCK}+ 75	-	2/F_{MCK} +113	ns
		1.8V≤EV_{DD}≤5.5V C=30pF Note1		-	2/F_{MCK}+ 100	-	2/F_{MCK} +150	ns

Note1: C is the load capacitance of the SCLKp and SDOp output lines.

Note: Through the port inputmode register and the port outputmode register, The SDIp pin and SCLKp pin are selected as the normal input buffer and the SDOp pin is selected as the normal output mode.

Remark: It is guaranteed by the design and not tested in mass production.

4) Four-wire SPI mode (slave mode, external clock input)

(T_A= -40~105℃, 1.8V≤EV_{DD}=V_{DD}≤5.5V, V_{SS}=EV_{SS}=0V)

Item	Symbol	Condition		-40 ~ 85℃		85 ~ 105℃		Unit
				Min	Max	Min	Max	
SSI00 set up time	T_{SSIK}	DAPmn=0	2.7V ≤ EV_{DD} ≤ 5.5V	120	-	240	-	ns
			1.8V ≤ EV_{DD} ≤ 5.5V	200	-	400	-	ns
		DAPmn=1	2.7V ≤ EV_{DD} ≤ 5.5V	1/F_{MCK}+120	-	1/F_{MCK}+240	-	ns
			1.8V ≤ EV_{DD} ≤ 5.5V	1/F_{MCK}+200	-	1/F_{MCK}+400	-	ns
SSI00 hold time	T_{KSSI}	DAPmn=0	2.7V ≤ EV_{DD} ≤ 5.5V	1/F_{MCK}+120	-	1/F_{MCK}+240	-	ns
			1.8V ≤ EV_{DD} ≤ 5.5V	1/F_{MCK}+200	-	1/F_{MCK}+400	-	ns
		DAPmn=1	2.7V ≤ EV_{DD} ≤ 5.5V	120	-	240	-	ns
			1.8V ≤ EV_{DD} ≤ 5.5V	200	-	400	-	ns

Note: Through the port inputmode register and the port outputmode register, The SDIp pin and SCLKp pin are selected as the normal input buffer and the SDOp pin is selected as the normal output mode.

Remark: It is guaranteed by the design and not tested in mass production.

5) Simple IIC mode

(T_A= -40~105℃, 1.8V≤EV_{DD}=V_{DD}≤5.5V, V_{SS}=EV_{SS}=0V)

Item	Symbol	Condition	-40 ~ 85℃		85 ~ 105℃		Unit
			Min	Max	Min	Max	
SCLr Clock frequency	F_{SCL}	2.7V ≤ EV_{DD} ≤ 5.5V C_b = 50 pF, R_b = 2.7 KΩ	-	1000 Note1	-	400Note1	KHz
		1.8V ≤ EV_{DD} ≤ 5.5V C_b = 100 pF, R_b = 3 KΩ	-	400 Note1	-	100Note1	KHz
		1.8V ≤ EV_{DD} ≤ 2.7V C_b = 100 pF, R_b = 5 KΩ	-	300 Note1	-	75Note1	KHz
Hold time when SCLr is low	T_{LOW}	2.7V ≤ EV_{DD} ≤ 5.5V C_b = 50 pF， R_b = 2.7 KΩ	475	-	1200	-	ns
		1.8V ≤ EV_{DD} ≤ 5.5V C_b = 100 pF， R_b = 3 KΩ	1150	-	4600	-	ns
		1.8V ≤ EV_{DD} ≤ 2.7V C_b = 100 pF, R_b = 5 KΩ	1550	-	6500	-	ns
Hold time when SCLr is high	T_{HIGH}	2.7V ≤ EV_{DD} ≤ 5.5V C_b = 50 pF, R_b = 2.7 KΩ	475	-	1200	-	ns
		1.8V ≤ EV_{DD} ≤ 5.5V C_b = 100 pF, R_b = 3 KΩ	1150	-	4600	-	ns
		1.8V ≤ EV_{DD} ≤ 2.7V C_b = 100 pF, R_b = 5 KΩ	1550	-	6500	-	ns
Data establishment time (received)	$T_{SU:DAT}$	2.7V ≤ EV_{DD} ≤ 5.5V C_b = 50 pF, R_b = 2.7 KΩ	1/F_{MCK}+85 Note 2	-	1/F_{MCK}+220 Note 2	-	ns
		1.8V ≤ EV_{DD} ≤ 5.5V C_b = 100 Pf, R_b = 3 KΩ	1/F_{MCK}+145 Note 2	-	1/F_{MCK}+580 Note 2	-	ns
		1.8V ≤ EV_{DD} ≤ 2.7V C_b = 100 pF, R_b = 5 KΩ	1/F_{MCK}+230 Note 2	-	1/F_{MCK}+1200 Note 2	-	ns
Data retention time (send)	$T_{HD:DAT}$	2.7V ≤ EV_{DD} ≤ 5.5V C_b = 50 pF, R_b = 2.7 KΩ	-	305	-	770	ns
		1.8V ≤ EV_{DD} ≤ 5.5V C_b = 100 pF, R_b = 3 KΩ	-	355	-	1420	ns
		1.8V ≤ EV_{DD} ≤ 2.7V C_b = 100 pF, R_b = 5 KΩ	-	405	-	2070	ns

Note1: Must be set to at least F_{MCK}/4.

Note2: The set value of F_{MCK} cannot exceed the holding time of SCLr= “L” and SCLr= “H”.

Remark: It is guaranteed by the design and not tested in mass production.

6.7.2 Serial Interface IICA

1) I²C standard mode

(T_A= -40~105℃, 1.8V≤EV_{DD}=V_{DD}≤5.5V, V_{SS}=EV_{SS}=0V)

Item	Symbol	Condition	Specification Value		Unit
			Min	Max	
SCLAr clock frequency	F_{SCL}	Standard mode: F_{CLK}≥1MHz	-	100	KHz
Start condition set up time	$T_{SU:STA}$	-	4.7	-	us
Start condition hold time Note1	$T_{HD:STA}$	-	4.0	-	us
Hold time when SCLAr is low	T_{LOW}	-	4.7	-	us
Hold time when SCLAr is high	T_{HIGH}	-	4.0	-	us
Data establishment time (received)	$T_{SU:DAT}$	-	250	-	ns
Data retention time (send)Note2	$T_{HD:DAT}$	-	0	3.45	us
Stop condition set up time	$T_{SU:STO}$	-	4.0	-	us
Bus idle time	T_{BUF}	-	4.7	-	us

Note1: Generate the first clock pulse after generating the start condition or restarting the condition.

Note2: During normal transmission, THD: the maximum value of DAT (MAX.) needs to be guaranteed, and it is necessary to wait for an acknowledgement (ACK).

Note: The MAX. value of Cb (communication line capacitance) of each mode and the value of Rb (communication line pull-up resistance value) at this time are as follows:

Standard mode: Cb=400pF, Rb=2.7kΩ

2) I²C fast mode

(T_A= -40~105℃, 1.8V≤EV_{DD}=V_{DD}≤5.5V, V_{SS}=EV_{SS}=0V)

Item	Symbol	Condition	Specification Value		Unit
			Min	Max	
SCLAr clock frequency	F_{SCL}	Fast mode: F_{CLK}≥3.5MHz	-	400	KHz
Start condition set up time	$T_{SU:STA}$	-	0.6	-	us
Start condition hold time Note1	$T_{HD:STA}$	-	0.6	-	us
Hold when SCLAr is low time	T_{LOW}	-	1.3	-	us
Hold when SCLAr is high time	T_{HIGH}	-	0.6	-	us
Data set up time (received)	$T_{SU:DAT}$	-	100	-	ns
Data hold time (send)Note2	$T_{HD:DAT}$	-	0	0.9	us
Stop condition set up time	$T_{SU:STO}$	-	0.6	-	us
Bus idle time	T_{BUF}	-	1.3	-	us

Note1: Generate the first clock pulse after generating the start condition or restarting the condition.

Note2: During normal transmission, tHD: the maximum value of DAT (MAX.) needs to be guaranteed, and it is necessary to wait for an acknowledgement (ACK)。

Note: The MAX. value of Cb (communication line capacitance) of each mode and the value of Rb (communication line pull-up resistance value) at this time are as follows:

Fast mode: Cb=320pF, Rb=1.1Kω

3) I²C enhanced fast mode

(T_A= -40~105℃, 1.8V≤EV_{DD}=V_{DD}≤5.5V, V_{SS}=EV_{SS}=0V)

Item	Symbol	Condition	Specification Value		Unit
			Min	Max	
SCLAr clock frequency	F_{SCL}	Enhanced fast mode: F_{CLK}≥10MHz	-	1000	KHz
Start condition set up time	$T_{SU:STA}$	-	0.26	-	us
Start condition hold time Note1	$T_{HD:STA}$	-	0.26	-	us
Hold time when SCLAr is low	T_{LOW}	-	0.5	-	us
When SCLAr is high hold time	T_{HIGH}	-	0.26	-	us
Data set up time (received)	$T_{SU:DAT}$	-	50	-	ns
Data hold time (send)Note2	$T_{HD:DAT}$	-	0	0.45	us
Stop condition set up time	$T_{SU:STO}$	-	0.26	-	us
Bus idle time	T_{BUF}	-	0.5	-	us

Note1: Generate the first clock pulse after generating the start condition or restarting the condition.

Note2: During normal transmission, tHD: the maximum value of DAT (MAX.) needs to be guaranteed, and it is necessary to wait for an acknowledgement (ACK).

Note: The MAX. value of Cb (communication line capacitance) of each mode and the value of Rb (communication line pull-up resistance value) at this time are as follows:

Enhanced fast mode: Cb=120pF, Rb=1.1kΩ

6.8 Analog Characteristic

6.8.1 A/D Converter Characteristic

The distinction of A/D converter characteristic

Reference voltage / Input channel	Reference voltage (+) =AV_{REFP} Reference voltage (-) =AV_{REFM}	Reference voltage (+) =V_{DD} Reference voltage (-) =V_{SS}
ANI0~ ANI20	See 6.8.1(1)。	See (2)。
Internal reference voltage, output voltage of temperature sensor		

1) Select the case of reference voltage (+)=AV_{REFP}/ANI0, reference voltage (-)=AV_{REFM}/ANI1 (T_A= -40~105℃, 1.8V≤AV_{REFP}≤EV_{DD}=V_{DD}≤5.5V, V_{SS}=0V, reference voltage (+)=AV_{REFP}, reference voltage (-)=AV_{REFM}=0V)

Item	Symbol	Condition		Min	Typ	Max	Unit
Resolution	RES	-		-	12	-	bit
Composite error Note 1	AINL	12-bit resolution	1.8V ≤AV_{REFP}≤ 5.5V	-	3	-	LSB
Zero error Note 1	E_{ZS}	12-bit resolution	1.8V ≤AV_{REFP}≤ 5.5V	-	0	-	LSB
Full scale error Note 1	E_{FS}	12-bit resolution	1.8V ≤AV_{REFP}≤ 5.5V	-	0	-	LSB
Integral linearity error Note 1	EL	12-bit resolution	1.8V ≤AV_{REFP}≤ 5.5V	-1	-	1	LSB
Differential linearity error Note 1	ED	12-bit resolution	1.8V ≤AV_{REFP}≤ 5.5V	-1.5	-	1.5	LSB
Conversion time Note 3	T_{CONV}	12-bit resolution Conversion object: ANI2~ ANI15	1.8V ≤V_{DD}≤ 5.5V	45	-	-	1/F_{ADC}
		12-bit resolution Conversion object: Internal reference voltage, The output voltage of the temperature sensor, PGA output voltage	1.8V ≤V_{DD}≤ 5.5V	72	-	-	1/F_{ADC}
External input resistance	R_{AIN}	R_{AIN} ＜ (Ts / (F_{ADC} x C_{ADC} x ln(2^{12+2})) - R_{ADC})		-	7.5 Note4	-	KΩ
Sampling switch resistance	R_{ADC}	-		-	-	1.5	KΩ
Sample holding capacitance	C_{ADC}	-		-	2	-	pF
Analog input voltage	V_{AIN}	ANI2~ ANI15		0	-	AV_{REFP}	V
		Internal reference voltage（1.8V≤V_{DD}≤5.5V）		V_{BGR} Note2			V
		The output voltage of the temperature sensor（1.8V≤V_{DD}≤5.5V）		V_{TMPS25} Note2			V

Note1: Does not include quantization error (±1/2 LSB).

Note2: Please refer to "6.8.2 Characteristic of Temperature Sensor/Internal Reference Voltage"。

Note3: F_{ADC} is the action frequency of AD. The maximum action frequency is 64MHz.

Note4: It is guaranteed by the design and not tested in mass production. The typical value is the calculated value under the condition of default sampling period Ts=13.5 and conversion speed F_{ADC}=64MHz.

2) Select the case of reference voltage (+)=V_{DD} and reference voltage (-)=V_{SS}
(T_A= -40~ 105℃, 1.8V≤ EV_{DD}= V_{DD}≤ 5.5V, V_{SS}=EV_{SS}=0V, reference voltage (+) =V_{DD}, reference voltage (-)=V_{SS})

Item	Symbol	Condition		Min	Typ	Max	Unit
Resolution	RES			-	12	-	bit
External input resistance	R_{AIN}	R_{AIN} < (Ts / (F_{AD} x C_{ADC} x ln(2^{12+2})) - R_{ADC})		-	7.5 Note4	-	KΩ
Sampling switch resistance	R_{ADC}			-		1.5	KΩ
Sample holding capacitance	C_{ADC}			-	2	-	pF
Composite error Note 1	AINL	12-bit resolution	1.8V≤AV_{REFP}≤5.5V	-	6	-	LSB
Conversion time Note 3	t_{CONV}	12-bit resolution Conversion object: ANI0～ANI15	1.8V≤V_{DD}≤5.5V	45	-	-	1/F_{ADC}
		12-bit resolution Conversion object: Internal reference voltage, The output voltage of the temperature sensor, PGA output voltage	1.8V≤V_{DD}≤5.5V	72	-	-	1/F_{ADC}
Zero error Note 1	E_{ZS}	12-bit resolution	1.8V≤AV_{REFP}≤5.5V	-	0	-	LSB
Full scale error Note 1	E_{FS}	12-bit resolution	1.8V≤AV_{REFP}≤5.5V	-	0	-	LSB
Integral linearity error Note 1	ILE	12-bit resolution	1.8V≤AV_{REFP}≤5.5V	-2	-	2	LSB
Differential linearity error Note 1	DLE	12-bit resolution	1.8V≤AV_{REFP}≤5.5V	-3	-	3	LSB
Analog input voltage	V_{AIN}	ANI0～ANI7		0	-	V_{DD}	V
		ANI8～ANI20		0	-	EV_{DD}	V
		Internal reference voltage （1.8V≤V_{DD}≤5.5V）		V_{BGR} Note2			V
		The output voltage of the temperature sensor （1.8V≤V_{DD}≤5.5V）		V_{TMPS25} Note2			V

Note1: Does not include quantization error (±1/2 LSB).

Note2: Please refer to "6.8.2 Characteristic of Temperature Sensor/Internal Reference Voltage"。

Note3: F_{ADC} is the action frequency of AD. The maximum action frequency is 64MHz.

Note4: It is guaranteed by the design and not tested in mass production. The typical value is the calculated value under the condition of default sampling period Ts=13.5 and conversion speed F_{ADC}=64MHz.

6.8.2 Characteristic of Temperature Sensor/Internal Reference Voltage

(T_A= -40~105℃, 1.8V≤V_{DD}≤5.5V, V_{SS}=EV_{SS}=0V)

Item	Symbol	Condition	Min	Typ	Max	Unit
The output voltage of the temperature sensor	V_{TMPS25}	T_A=25℃	-	1.09	-	V
Internal reference voltage Temperature Coefficient	V_{BGR}	T_A= -40~10℃	1.25	1.45	1.65	V
		T_A=10~70℃	1.38	1.45	1.50	V
		T_A=70~105℃	1.32	1.45	1.55	V
The output voltage of the temperature sensor	F_{VTMPS}	-	-	-3.5	-	mV/℃
Internal reference voltage	T_{AMP}	-	5	-	-	us

6.8.3 D/A Converter

(T_A= -40~105℃, 1.8V≤EV_{DD}=V_{DD}≤5.5V, V_{SS}=EV_{SS}=0V)

Item	Symbol	Condition		Min	Typ	Max	Unit
Resolution	RES	-	-	-	-	8	bit
Composite error	ET	Rload=4MΩ	1.8V≤V_{DD}≤5.5V	-2.5	-	2.5	LSB
Stable schedule	T_{SET}	Cload=20pF	2.7V≤V_{DD}≤5.5V	-	-	3	us
			1.8V≤V_{DD}<2.7V	-	-	6	us
Output impedance	RO	Rload=4MΩ	2.0V≤V_{DD}≤5.5V	4.7	-	8	KΩ

6.8.4 Comparator

(T_A= -40~105℃, 1.8V≤EV_{DD}=V_{DD}≤5.5V, V_{SS}=EV_{SS}=0V)

Item	Symbol	Condition		Min	Typ	Max	Unit
Input offset voltage	V_{OFFSET}	-		-	±10	± 40	mV
input voltage range	V_{IN}	-		0	-	V_{DD}	V
Internal reference voltage deviation	ΔV_{IREF}	CmRVM register: 7FH~80H (m = 0， 1)		-	-	±2	LSB
		others		-	-	±1	LSB
Response time	T_{CR}, T_{CF}	input amplitude ±100mV		-	70	150	ns
Stable operation time[Note1]	T_{STB}	CMPn=0->1	V_{DD}=3.3~5.5V	-	-	1	us
			V_{DD}=1.8~3.3V	-	-	3	
Reference voltage stabilization time	T_{VR}	CVRE=0->1 [Note2]		-	-	20	us
operating current	I_{CMPDD}	Refer to 6.5.2 Power Supply Current Characteristics					

Note1: The time required from the enable of the comparator action (CMPnEN=0 —>1) to meeting the various DC/AC style requirements of CMP.

Note2: After the internal reference voltage generator is enabled (by setting the CVREm bit to 1; m = 0 to 1), the comparator output can be enabled after the reference voltage stabilization time (CnOE bit = 1; n = 0 to 1)

6.8.5 Programmable Gain Amplifier PGA

(T_A= -40~105℃, 1.8V≤EV_{DD}=V_{DD}≤5.5V, V_{SS}=EV_{SS}=0V)

Symbol	Parameter	Condition		Min	Typ	Max	Unit
Input deviation voltage	V_{IOPGA}	-		-	-	±10	mV
Input voltage range	V_{IPGA}	-		0	-	0.9xV_{DD}/Gain	V
Output voltage range	V_{IOHPGA}	-		0.93xV_{DD}	-	-	V
	V_{IOLPGA}	-		-	-	0.07xV_{DD}	V
Gain deviation	-	x4	-	-	-	±1	%
		x8	-	-	-	±1	%
		x10	-	-	-	±1	%
		x12	-	-	-	±2	%
		x14	-	-	-	±2	%
		x16	-	-	-	±2	%
		x32	-	-	-	±3	%
Conversion rate Note 2	SR_{RPGA}	rise Vin= 0.1V_{DD}/gain to 0.9V_{DD}/gain. 10 to 90% of output voltage amplitude	4.0V≤V_{DD}≤5.5V (Other than x32)	3.5	-	-	V/us
			4.0V≤V_{DD}≤5.5V (x32)	3.0	-	-	
			1.8V≤V_{DD}≤4.0V	0.5	-	-	
	SR_{FPGA}	drop Vin= 0.1V_{DD}/gain to 0.9V_{DD}/gain. 90 to 10% of output voltage amplitude	4.0V≤V_{DD}≤5.5V (Other than x32)	3.5	-	-	
			4.0V≤V_{DD}≤5.5V (x32)	3.0	-		
			1.8V≤V_{DD}≤4.0V	0.5	-	-	
Stable operation time Note 1	T_{PGA}	x4	-	-	-	5	us
		x8	-	-	-	5	us
		x10	-	-	-	5	us
		x12	-	-	-	10	us
		x14	-	-	-	10	us
		x16	-	-	-	10	us
		x32	-	-	-	10	us
Working current	I_{PGADD}	Refer to 6.5.2 Power Supply Current Characteristics					

Note1: The time required from PGA action enable (PGAEN=1) to meeting various DC and AC style requirements of PGA.

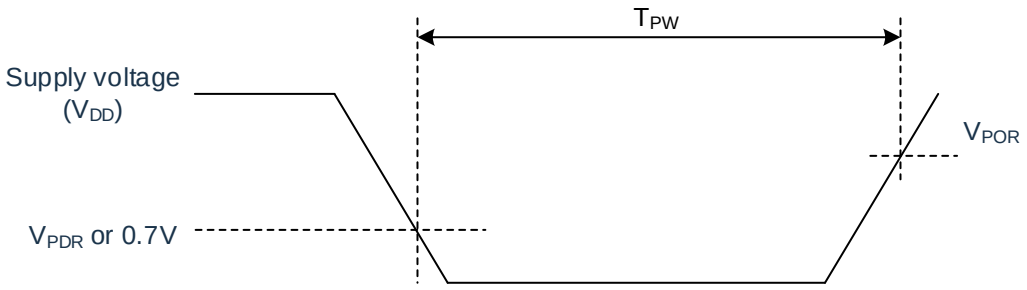
Note2: It is guaranteed by the design and not tested in mass production.

6.8.6 POR Circuit Characteristic

(T_A= -40~105℃, V_{SS}=0V)

Item	Symbol	Condition	Min	Typ	Max	Unit
Detection voltage	V_{POR}	When the power supply voltage rises	-	1.50	1.75	V
	V_{PDR}	When the power supply voltage drops	1.37	1.45	-	V
Minimum pulse width[Note1]	T_{PW}	-	300	-	-	us

Note1: This is the time required for POR to reset when V_{DD} is lower than V_{PDR}. In addition, in the deep sleep mode, when the main system clock (F_{MAIN}) is stopped by setting bit0 (HIOSTOP) and bit7 (MSTOP) of the clock operation status control register (CSC), the oscillation of the main system clock (F_{MAIN}) is stopped from V_{DD} lower than 0.7V to rise above V_{POR}. Time required for POR reset.



6.8.7 LVD Circuit Characteristic

1. Reset mode, interrupt mode

(T_A= -40~105℃, V_{PDR}≤V_{DD}≤5.5V, V_{SS}=0V)

Item	Symbol	Condition	Min	Typ	Max	Unit
Detection voltage	V_{LVD0}	power supply voltage rises	-	4.06	4.26	V
		power supply voltage drops	3.78	3.98	-	V
	V_{LVD1}	power supply voltage rises	-	3.75	-	V
		power supply voltage drops	-	3.67	-	V
	V_{LVD2}	power supply voltage rises	-	3.13	-	V
		power supply voltage drops	-	3.06	-	V
	V_{LVD3}	power supply voltage rises	-	3.02	-	V
		power supply voltage drops	-	2.96	-	V
	V_{LVD4}	power supply voltage rises	-	2.92	-	V
		power supply voltage drops	-	2.86	-	V
	V_{LVD5}	power supply voltage rises	-	2.81	-	V
		power supply voltage drops	-	2.75	-	V
	V_{LVD6}	power supply voltage rises	-	2.71	-	V
		power supply voltage drops	-	2.65	-	V
	V_{LVD7}	power supply voltage rises	-	2.61	-	V
		power supply voltage drops	-	2.55	-	V
	V_{LVD8}	power supply voltage rises	-	2.50	-	V
		power supply voltage drops	-	2.45	-	V
	V_{LVD9}	power supply voltage rises	-	2.09	-	V
		power supply voltage drops	-	2.04	-	V
	V_{LVD10}	power supply voltage rises	-	1.98	-	V
		power supply voltage drops	-	1.94	-	V
	V_{LVD11}	power supply voltage rises	-	1.88	1.98	V
		power supply voltage drops	1.75	1.84	-	V
Minimum pulse width	T_{LW}	-	300	-	-	us
Detection delay	-	-	-	-	300	us

2. Interrupt & reset mode

(T_A= -40~105℃, V_{PDR} ≤V_{DD}≤5.5V, V_{SS}=0V)

Item	Symbol	Condition			Min	Typ	Max	Unit
Interrupt & reset mode	V_{LVDA0}	V_{POC2}=0 V_{POC1}=0 V_{POC0}=0	Decrease reset voltage		1.60	1.63	-	V
	V_{LVDA1}		LVIS1=1 LVIS0=0	rising reset release voltage	-	1.77	1.81	V
				drop interrupt voltage	1.70	1.73	-	V
	V_{LVDA2}		LVIS1=0 LVIS0=1	rising reset release voltage	-	1.88	-	V
				drop interrupt voltage	-	1.84	-	V
	V_{LVDA3}		LVIS1=0 LVIS0=0	rising reset release voltage	-	2.92	-	V
				drop interrupt voltage	-	2.86	-	V
	V_{LVDB0}	V_{POC2}=0 V_{POC1}=0 V_{POC0}=1	Decrease reset voltage		-	1.84	-	V
	V_{LVDB1}		LVIS1=1 LVIS0=0	rising reset release voltage	-	1.98	-	V
				drop interrupt voltage	-	1.94	-	V
	V_{LVDB2}		LVIS1=0 LVIS0=1	rising reset release voltage	-	2.09	-	V
				drop interrupt voltage	-	2.04	-	V
	V_{LVDB3}		LVIS1=0 LVIS0=0	rising reset release voltage	-	3.13	-	V
				drop interrupt voltage	-	3.06	-	V
	V_{LVDC0}	V_{POC2}=0 V_{POC1}=1 V_{POC0}=0	Decrease reset voltage		-	2.45	-	V
	V_{LVDC1}		LVIS1=1 LVIS0=0	rising reset release voltage	-	2.61		V
				drop interrupt voltage	-	2.55	-	V
	V_{LVDC2}		LVIS1=0 LVIS0=1	rising reset release voltage	-	2.71	-	V
				drop interrupt voltage	-	2.65	-	V
	V_{LVDC3}		LVIS1=0 LVIS0=0	rising reset release voltage	-	3.75	-	V
				drop interrupt voltage	-	3.67	-	V
	V_{LVDD0}	V_{POC2}=0 V_{POC1}=1 V_{POC0}=1	Decrease reset voltage		-	2.75	-	V
	V_{LVDD1}		LVIS1=1 LVIS0=0	rising reset release voltage	-	2.92	-	V
				drop interrupt voltage	-	2.86	-	V
	V_{LVDD2}		LVIS1=0 LVIS0=1	rising reset release voltage	-	3.02	-	V
				drop interrupt voltage	-	2.96	-	V
	V_{LVDD3}		LVIS1=0 LVIS0=0	rising reset release voltage	-	4.06	4.14	V
				drop interrupt voltage	3.90	3.98	-	V

Remark: It is guaranteed by the design and not tested in mass production.

6.8.8 The Rising Slope of The Power Supply Voltage Characteristic

(T_A= -40~105℃, V_{SS}=0V)

Item	Symbol	Condition	Min	Typ	Max	Unit
Reset time	T_{RESET}	-	-	2	-	ms
The rising slope of the power supply voltage	S_{VDD}	-	-	-	54	V/ms

Remark: It is guaranteed by the design and not tested in mass production.

6.9 Memory Characteristic

6.9.1 Flash Memory Characteristic

(T_A= -40~105℃, 1.8V≤EV_{DD}=V_{DD}≤5.5V, V_{SS}=EV_{SS}=0V)

Symbol	Parameter	Conditions	Min	Max	Unit
T_{PROG}	Word Program(32bit)	T_A= -40~105℃	24	30	us
T_{ERASE}	Sector erase(512B)	T_A= -40~105℃	4	5	ms
	Chip erase	T_A= -40~105℃	20	40	ms
N_{END}	Endurance	T_A= -40~105℃	20	-	kcycles
T_{RET}	Data retention	20 kcycles[Note1] at T_A = 105℃	20	-	Years

Note1: Cycling performed over the whole temperature range.

Remark: It is guaranteed by the design and not tested in mass production.

6.9.2 RAM Memory Characteristic

(T_A= -40~105℃, 1.8V≤EV_{DD}=V_{DD}≤5.5V, V_{SS}=EV_{SS}=0V)

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{ramhold}$	RAM Hold Voltage	T_A= -40~105℃	0.8	-	V

Remark: It is guaranteed by the design and not tested in mass production.

6.10 Electrical Sensitivity Characteristic

6.10.1 Electrostatic Discharge (ESD) Characteristic

Symbol	Parameter	Conditions	Class
$V_{ESD(HBM)}$	Electrostatic discharge voltage (human body model)	T_A = 25˚C conforming to JESD22-A114	3A

Remark: It is guaranteed by the design and not tested in mass production.

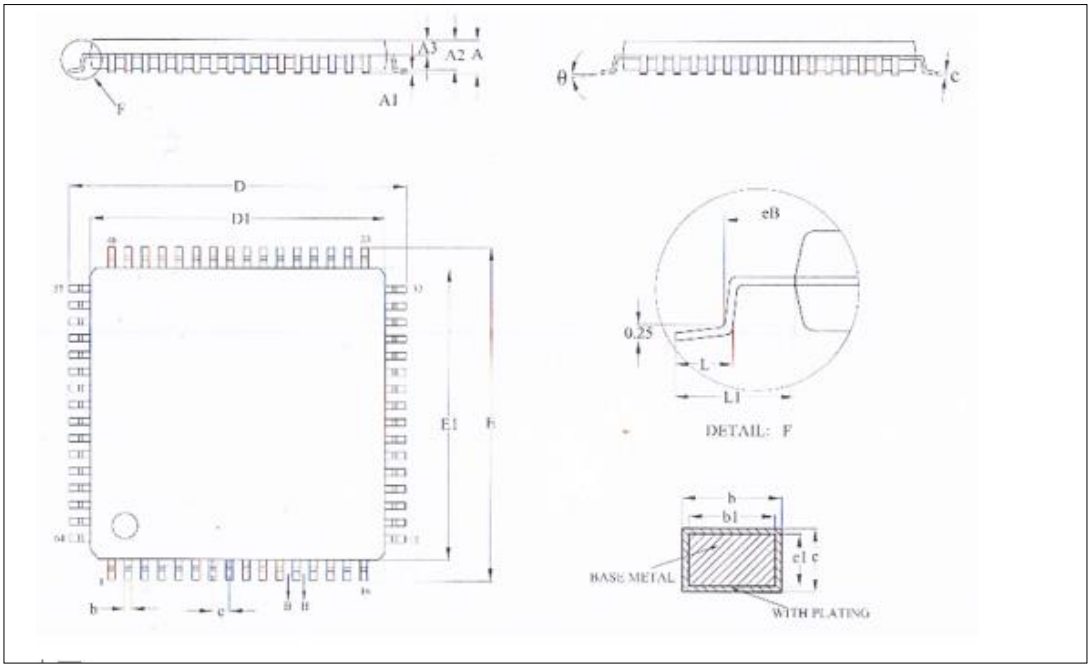
6.10.2 Static Latch-up (LU) Characteristic

Symbol	Parameter	Conditions	Class
LU	Static latch-up class	T_A = 25˚C conforming to JESD78E	I levelA

Remark: It is guaranteed by the design and not tested in mass production.

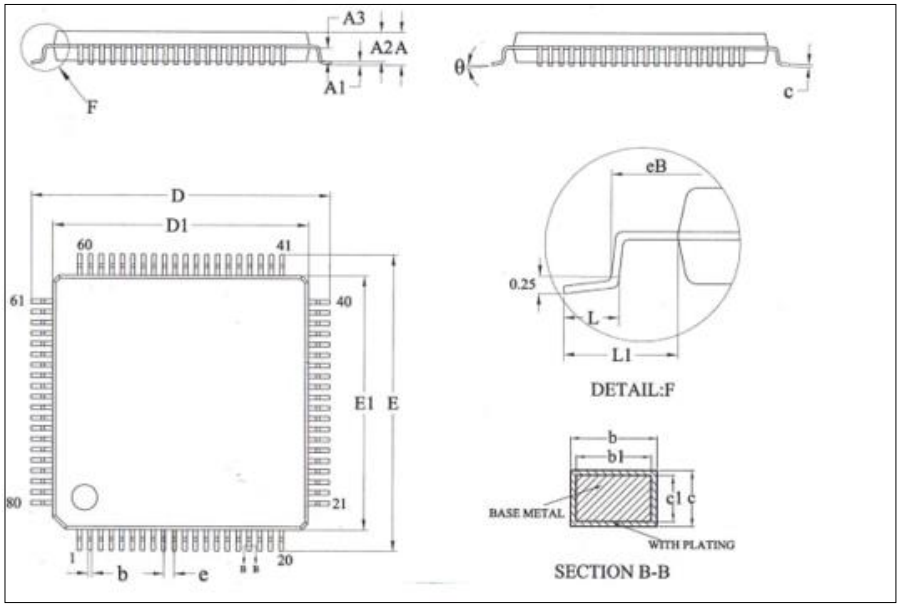
7 Package Size Chart

7.1 LQFP64 (7x7mm, 0.4mm)



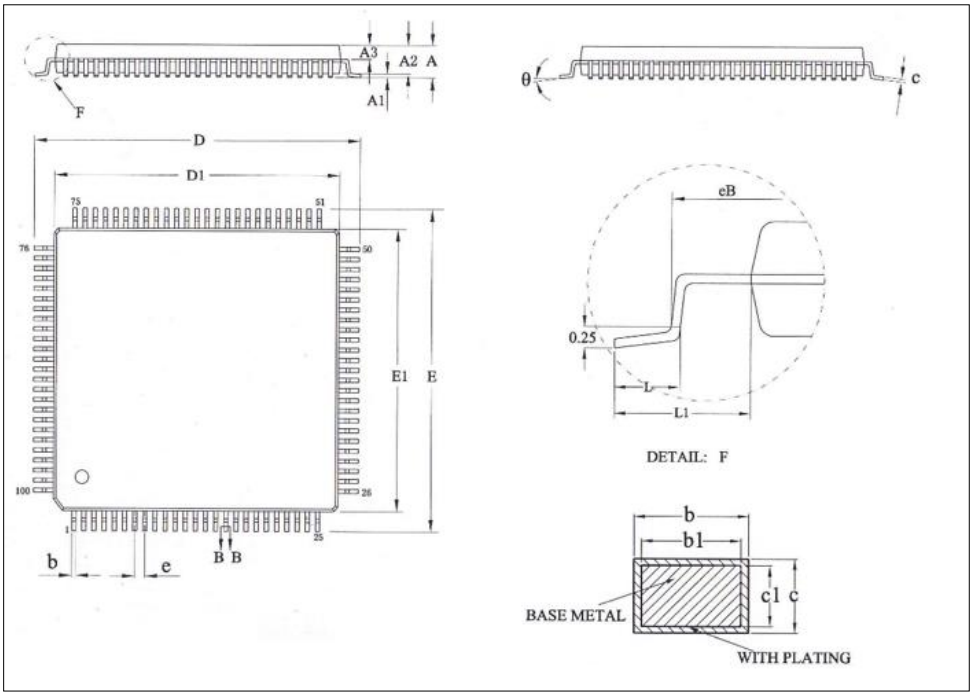
Symbol	Millimeter		
	Min	Nom	Max
A	-	-	1.60
A1	0.05	-	0.15
A2	1.35	1.40	1.45
A3	0.59	0.64	0.69
b	0.16	-	0.24
b1	0.15	0.18	0.21
c	0.13	-	0.17
c1	0.12	0.13	0.14
D	8.80	9.00	9.20
D1	6.90	7.00	7.10
E	8.80	9.00	9.20
E1	6.90	7.00	7.10
eB	8.10	-	8.25
e	0.40BSC		
L	0.45	-	0.75
L1	1.00REF		
θ	0	-	7°

7.2 LQFP80 (12×12mm, 0.5mm)



Symbol	Millimeter		
	Min	Nom	Max
A	-	-	1.60
A1	0.05	-	0.15
A2	1.35	1.40	1.45
A3	0.59	0.64	0.69
b	0.18	-	0.26
b1	0.17	0.20	0.23
c	0.13	-	0.17
c1	0.12	0.13	0.14
D	13.80	14.00	14.20
D1	11.90	12.00	12.10
E	13.80	14.00	14.20
E1	11.90	12.00	12.10
eB	13.05	-	13.25
e	0.50BSC		
L	0.45	0.60	0.75
L1	1.00REF		
θ	0	-	7°

7.3 LQFP100 (14x14mm，0.5mm)



Symbol	Millimeter		
	Min	Nom	Max
A	-	-	1.60
A1	0.05	-	0.15
A2	1.35	1.40	1.45
A3	0.59	0.64	0.69
b	0.18	-	0.26
b1	0.17	0.20	0.23
c	0.13	-	0.17
c1	0.12	0.13	0.14
D	15.80	16.00	16.20
D1	13.90	14.00	14.10
E	15.80	16.00	16.20
E1	13.90	14.00	14.10
eB	15.05	-	15.35
e	0.50BSC		
L	0.45	-	0.75
L1	1.00REF		
θ	0	-	7°

8 Revision History

Revision	Date	Modify content
V1.0	Dec 2021	Initial verison
V1.0.3	Feb 2023	1) Correction function I/O port; 2) 1.1 Correct deep sleep power consumption; 3) 1.2 Add product selection table; 4) Adjust the electrical characteristic parameters in chapters 6.4.1, 6.4.2, 6.4.3, 6.5.1, 6.5.2, 6.8.1, 6.8.2, 6.8.3, 6.8.4, 6.8.6, 6.8.7, 6.8.8; 5) Correct the product pin function in section 1.3.3 and 4.1; 6) Description of contents in optimization chapters 1.3, 6.9, 6.10; 7) Manual format optimization.
V1.0.4	Mar 2023	1) Correct the 100pin multiplexing function 2) 1.3.2, 1.3.3, 4.1.2, 4.1.3 P137 Pin function SI00 corrected to SDI00
V1.0.5	Sep 2023	1) Modified1.1Introduction 2) Adjusted the format of the pinout diagram 3) P40 increase of 100pin, 80pin package diagram (TXD0) 4) Update P150~P156 pin characteristics in 6.2,6.3,6.5.1
V1.0.6	Nov 2023	Updated Flash erase times in 6.9.1